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ELECTRICAL CHARACTERISTICS OF METAL/*p*-TYPE CdTe SCHOTTKY CONTACTS*

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The Schottky barrier height of Al, Mg and Ag on chemically prepared *p*-type surface were measured with *I–V* techniques. The barrier heights were found to be independent of metal used, and equal to 0.73 ± 0.02 eV.

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Introduction

Cadmiun Telluride, which has a direct band gap of 1.54 eV has been recognized for some time as an attractive element for photovoltaic energy conversion. The barrier height on *n*-type CdTe has been investigated both on chemically etched [1–4] and cleaved surface [4–7] with a range of metal overlayers, but only a few papers have been devoted to Schottky barriers on *p*-type material [1, 2, 7].

In this paper, we report on investigations of electrical characteristics of the Al, Mg and Ag/CdTe junctions made on *p*-type material. Diode characteristics were studied by current–voltage measurements at room temperature.

Experimental

Single crystalline *p*-type CdTe wafers with resistivity of about 100 Ωcm were used as substrates. The substrates were etched in 5% Br-methanol solution for 5 min at room temperature, and rinsed with methanol. The metals were deposited by thermal evaporation through a metal mask with openings of 0.75 mm^2 in area. An ohmic contact was formed on the back side of the wafer by Au evaporation. Forward-bias current–voltage (*I–V*) measurements were carried out to obtain Schottky barrier heights (Φ_B) and ideality factor (n).

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Results

For Al, Ag and Mg in the as-deposited state the ideality factors n were very poor, being about 1.5. To improve the I–V characteristics the diodes were subjected to rapid thermal annealing (RTA) in vacuum (10^{-5} Torr) in temperature 400° C for Al and Ag, and 200° C for Mg. Annealing improved substantially the ideality factor to the value of $n = 1.05 \div 1.15$ for Al and $n = 1.2$ for Mg and Ag, leaving the value of saturation current nearly unchanged. Figure 1 illustrates typical I–V characteristic of annealed diodes. The bowing at higher current is attributed to a voltage dropping on a series resistance.

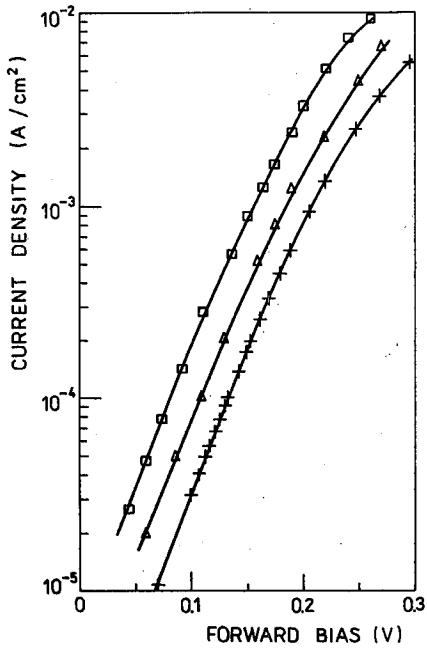

Fig. 1. The typical current–voltage characteristic for Al (+), Mg (Δ) and Ag (□) on p-type CdTe after rapid thermal annealing.

As the diodes have the ideality factors close to unity the I–V characteristics of annealed junctions could be analyzed in terms of the thermoionic-emission model of Schottky barrier current transport [8]. Within an experimental error the Schottky barrier heights for Al, Mg and Ag were determined to be the same and equal to 0.73 ∓ 0.03 eV. The results are in good agreement with the values obtained in [1] and about 0.1 eV greater than obtained in [2].

Discussion

The interface layer on Br-methanol etching CdTe is believed to be mixture of Te and oxidized tellurium [6, 7]. This interfacial layer may cause significant departure of n from unity [9] and leads to the poor I–V characteristics found prior to annealing. The I–V characteristics of diodes examined here were improved upon moderate thermal annealing; the ideality factor approached unity. This fact suggests that annealing leads to a drastic reduction of the interface layer, which may allow the metal to make an intimate contact with CdTe surface, improving the ideality of Schottky barrier or the defects acting as recombination centers were thermally annealed out or consumed by reaction with metals.

The unified model for Schottky barrier formation states that the Fermi level is pinned by the intrinsic defects introduced in the vicinity of the surface of a semiconductor [10]. On the basis of this model the barrier height is independent of the metal used. In our measurements of the three metals on p-type CdTe, the barrier heights are the same, thought Mg and Ag or Al differ in work function about 0.6 eV. No correlation between the barrier heights and the work function of the metal used was found. This agrees with unified defect model. That means that Fermi level is pined to states on CdTe surface located around 0.73 eV above the top of valence band. The existence of such a level has been reported in [11] (E_V+0.75 eV) and [12] (E_V+0.8 eV).

In conclusion the poor performance in the I–V characteristics in as-deposited states may be contributed to the defects in the vicinity of the interface during chemical etching. These defects were partially removed by moderate annealing. After the annealing Fermi-level pinning takes place and the level is independent of the deposited metal, being 0.73 eV above the top of valence band.

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