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Band-to-Band Tunneling Spectroscopy of Energy States in Ultrathin Silicon-on-Insulator p–n Diodes

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This study investigates the possible impact of the dopant distribution on the electrical characteristics of silicon-on-insulator p–n diodes with varying nanostructure widths. The devices were fabricated using rapid thermal annealing and electron-beam lithography, with the p–n junction formed in a region codoped with boron (B) acceptors and phosphorus (P) donors. Electrical measurements conducted at low temperatures reveal significant differences in electronic transport behavior for different widths, especially within the negative differential conductance region. The findings suggest that the band-to-band tunneling is strongly influenced by the dopant (impurity) and/or defect levels in the depletion layer, with a narrower device showing a pronounced dependence on the substrate voltage.

topics: Esaki diode, silicon-on-insulator, p–n junction, band-to-band tunneling

1. Introduction

As an extension of Moore's law [1] followed for decades until transistor miniaturization in nanoscale dimensions, the effects of dopant atoms on nanoscale Si MOSFETs (metal-oxide-semiconductor field-effect transistors) have been extensively studied, typically focusing on how non-uniform doping distribution influences the threshold characteristics of devices [2]. Precise control of doping has been shown to reduce fluctuations in threshold voltage [3]. Individual (discrete) dopants have also been demonstrated to contribute to single-electron tunneling transport [4–7] as quantum dots (QDs). Our group has even shown that clusters of dopants can introduce deep energy levels, potentially separating single-electron tunneling from thermally activated transport [8–10]. In nanoscale p–n diodes and Esaki diodes (highly doped p–n diodes) as well, dopant individuality and clustering are also expected to play significant roles. Therefore, a novel approach is required to provide more clarification on the relationship between the randomness of dopant distribution and transport mechanisms, especially in nanoscale p–n junctions, which are the basic structures of Esaki diodes.

Previous research on band-to-band tunneling (BTBT) in p–n diodes fabricated using silicon-on-insulator (SOI), with a width estimated to be on the order of 200 nm [11], suggested that QDs formed by random distributions of phosphorus (P) donors and boron (B) acceptors may contribute to dopant-mediated BTBT [12] or even to single-charge BTBT transport [13]. However, in nanowire p–n diodes subjected to rapid thermal annealing (RTA) for the drive-in doping process, a short heating time of approximately 20 s resulted in a very low yield of the devices as tunnel diodes, indicating potential issues with doping or etching, particularly in the codoped region which is most critical for the device operation. This study aims to investigate codoped regions in SOI devices with thin films through electrical characterization.

Tunnel diodes, also known as Esaki diodes, after L. Esaki, who first demonstrated them in Ge in 1958 [14] and Si in 1960 [15], are formed from p–n junctions where both the p-type and n-type regions are heavily doped ($N \gg N_{\mathrm{MIT}}$), resulting in Fermi energies lying within the bands. A key feature of tunnel diodes is that electron transport occurs by quantum mechanical tunneling, which depends on the operating bias state.

The energy band diagram of an Esaki diode in equilibrium shows that, in reverse bias ($V < 0$), the current increases monotonically, resulting in a relatively high current compared to regular p–n diodes. In forward bias ($V > 0$), the current reaches a maximum value (peak current I_{p}) and then decreases to a minimum value (valley current I_{v}), forming a region of negative differential conductance (NDC). Typically, due to the indirect-bandgap nature of Si, the BTBT transport in the NDC region is assisted by phonons for momentum conservation [16].

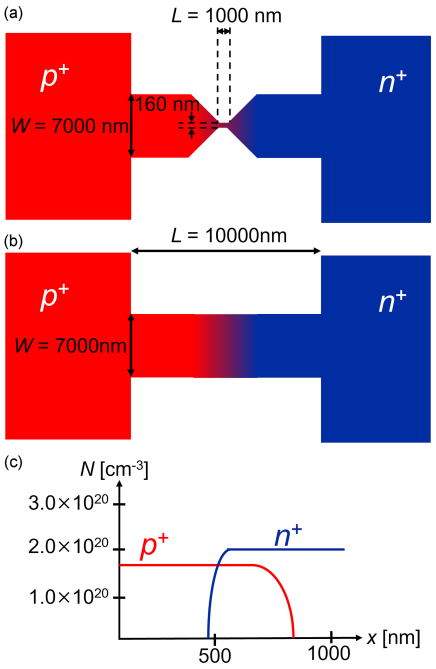

Fig. 1. (a) Schematic device structure of an SOI-based Esaki diode. (b) Illustration of doping profiles for N_D (doping with P-donors) and N_A (doping with B-acceptors), showing also the overlap which is a codoped region.

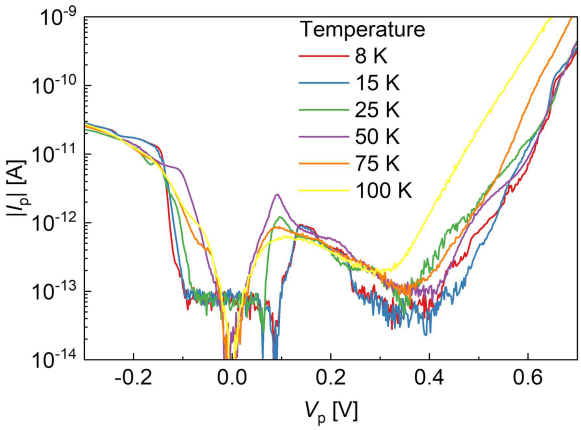

Fig. 2. I_p–V_p characteristics for a device with the nano-patterned central region with design width 160 nm, as a function of temperature in the range 8–100 K. Negative differential conductance (NDC) peak can be observed clearly even at 100 K.

Current transport in forward bias can be attributed to three main transport mechanisms [17]: (i) band-to-band tunneling; (ii) excess current; (iii) thermally-activated current. For tunneling to occur, energy states in the emitter must be occupied, while energy states in the collector must be unoccupied (available), the tunneling barrier must be small, and momentum must be conserved during band-to-band tunneling. Understanding electron transport mechanisms in low-dimensional Esaki diodes is crucial, as new physical phenomena and statistical interpretations are expected to emerge in such scales. These issues will be explored in the following sections.

2. Device structure and experimental results

2.1. Device fabrication and parameters

As illustrated in Fig. 1, the devices under study here are silicon-on-insulator (SOI) lateral diodes.

We will focus on the ones in which there is an overlap between the P-doping and B-doping areas (i.e., codoped region). P-donors and B-acceptors were added successively as impurities at high concentrations using a rapid thermal annealing (RTA) process. The left side is p and the right side is n, with doping concentrations estimated from four-point probe measurements on reference samples of 1.5×10^{20} cm^{-3}, and 2.2×10^{20} cm^{-3}, respectively.

The device sizes are designed as follows: (i) for the non-etched sample, the nanostructure length $L = 10000$ nm and the width $W = 7000$ nm; (ii) for the etched sample, the nanostructure length $L = 1000$ nm and the width $W = 160$ nm (for the narrowest section of the central part). Finally, it should be mentioned that the thickness of the top Si layer is approximately 20–30 nm, depending also on the region of the device. Fabrication of such nanoscale Esaki diodes presents a variety of challenges outlined elsewhere [18].

2.2. Experimental results

This section discusses the results of electrical measurements, focusing on the I_p–V_p characteristics of the devices mentioned above. Measurements were conducted from low temperatures (8.3 K) up to elevated temperatures of 100 K, while also monitoring the dependence on the substrate voltage (V_{sub}). The sample was introduced into a vacuum prober (GRAIL 10-305-4-LV-6H, Nagase Engineering Co., Ltd.), the chamber was evacuated, and the temperature was lowered to 8.3 K. Current–voltage measurements were performed using a semiconductor parameter analyzer (Agilent 4156C, Keysight Technologies).

Figure 2 shows the I_p–V_p characteristics of a device with a nanostructure nominal width of 160 nm. An NDC peak is observed around $V_p = 100$ mV.

A current dip beyond the peak indicates negative resistance, a feature observed in all six measurements from 8 to even 100 K, with minor variations in peak shape. Notably, the observation of NDC peaks at such an elevated temperature of 100 K is quite unique in our devices [11–13], in which

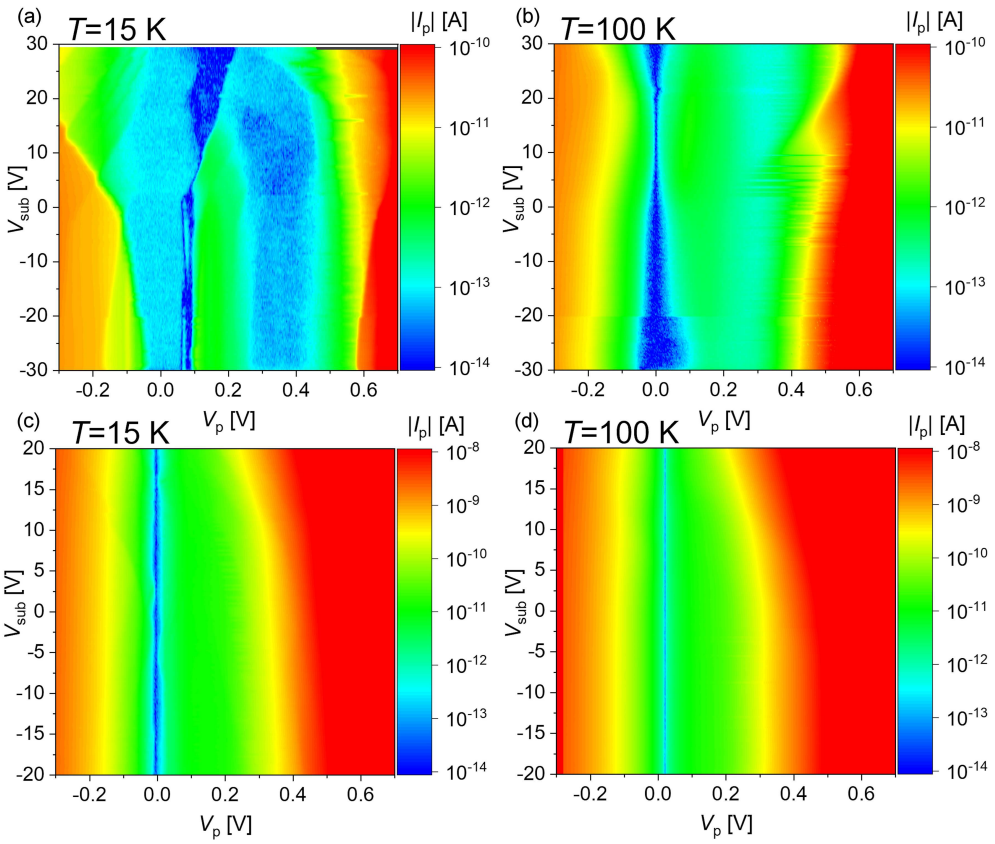

Fig. 3. I_p–V_p measured as a function of V_{sub} for different temperatures (here shown (a), (c) 15 K and (b), (d) 100 K) for devices with different design widths: (a), (b) 160 nm (nano-patterned device); (c), (d) 7000 nm (a reference large device without nano-patterning).

the excess current through deep-level gap states and thermally-activated current components usually hide the BTBT feature.

Figure 3 shows the I_p–V_p–V_{sub} characteristics (contour plots of $|I_p|$ in the space defined by V_p and V_{sub}) for the two devices under comparison, one with a nominal width of 160 nm (panels (a) and (b)) and one with a nominal width of 7000 nm (panels (c) and (d)) at temperatures of 15 K (see Fig. 3a and c) and 100 K (see Fig. 3b and d). At 15 K, a current increase near 0 mV is observed when a reverse bias is applied, which is one of the features of Esaki diode characteristics. In forward bias, the current exhibits a valley or a plateau in the range of V_p = 100–300 mV, which is indicative of the NDC region of an Esaki diode. The NDC peak observed earlier at low temperatures (8–50 K) was confirmed thus even at 100 K, which is a significantly higher temperature range than reported before.

As shown in Fig. 3, the effect of V_{sub} was also examined for each temperature value, with V_{sub} varied from −20 to 20 V in 250 mV increments during the measurements. To avoid resistance changes due to recontacting the probes on the electrodes, the probes were not lifted during the entire set of measurements.

3. Discussion

In this section, we explore the electronic transport mechanisms for devices with different widths that can explain the differences in behavior. The nano-patterned device exhibits typical features of an Esaki diode, but the yield is relatively low. The non-patterned device also exhibits features resembling Esaki diodes, but with a less pronounced NDC peak in forward bias.

A first model that can be considered focuses on differences in fabrication processes, especially related to impurity doping and nanostructure patterning. For the large device, a microstructure with a width of 7000 nm and a length of 10000 nm is first created, followed by impurity doping. This is also the case for the smaller device, but the microstructure is subsequently patterned to have different widths and a length of 1000 nm using an electron-beam lithography technique and reactive ion etching (RIE).

The concentration and distribution of impurities (dopants) are critical for device operation. Here, the doping was conducted using rapid thermal annealing (RTA) at 1050°C for a time of approximately 20 s in nitrogen (N_2) atmosphere. Due to

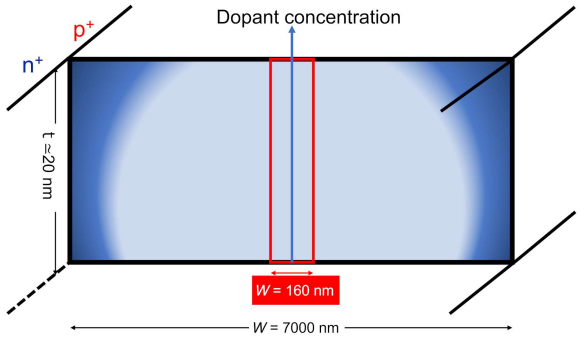

Fig. 4. Schematic representation (not to scale) of the edge effect, i.e., the occurrence of heavily-doped edges for the microstructure. The highly doped edges are removed by nano-patterning (etching) for the device with a design width of 160 nm. Color gradient is used to indicate the concentration gradient in the device.

this short-time processing, a concentration gradient may be induced within the microstructure, with a higher concentration expected to be obtained especially at the edges compared to the central area, as schematically illustrated in Fig. 4.

For the device with a design width of 160 nm, etching of the edges of the microstructure minimizes the influence of such heavily-doped regions, leading to a relatively low concentration in the central area. This may justify the relatively low yield of nano-patterned devices such as Esaki diodes. In contrast, for the device with a design width of 7000 nm, which does not require nano-patterning, the heavily-doped regions remain at the edges of the microstructure. Since the current is several orders of magnitude higher for this device than for the 160-nm devices, this suggests that charge transport is predominantly governed by the heavily-doped edges of the microstructure.

A second model considers the nanoscale dimensions of the narrower device. For the device with a design width of 160 nm, which lacks the heavily-doped edges due to etching required to form the nanostructure, a strong dependence on V_{sub} was observed, suggesting that impurity levels (or defect levels) within the depletion influence the BTBT current. The substrate voltage V_{sub} likely affects the band tails and energy levels within the depletion layer, but not as much the heavily-doped p and n regions of the device. The observed modulation of the BTBT current with varying V_{sub} suggests thus the importance of the gap states in transport. In the device with a design width of 7000 nm, there is a large number of dopants (both donors and acceptors) within the depletion layer, which may result in a weak dependence due to the compensation effect between many P-donors and B-acceptors, or due to the dominant influence of the heavily-doped regions at the edges of the microstructure. However, the fact that the device with a design width of 160 nm effectively contains a nanoscale structure in the center may also mean that deeper energy states are formed [19, 20] due to phenomena such as quantum-size effect or dielectric confinement effect [21, 22], thus further justifying the V_{sub} dependence, as observed in Fig. 3a and b.

Finally, there is another possible model that can explain the results. This model considers the presence of a non-uniform dopant distribution at the p–n junction interface resulting in dopant clusters, which can affect the dependence on V_{sub} as well. This is particularly important in nanoscale devices, in which a small number of dopant clusters. A strong electric field generated by V_{sub} can vary due to this non-uniformity, causing variations in current at that V_{sub}. As mentioned above, for the narrower device, the limited number of dopant clusters within this small volume may lead to significant V_{sub} influence, causing the observed current variations.

Further systematic analysis is necessary to clarify which mechanism is dominant for the interpretation of the overall behavior of these devices.

4. Conclusions

This study investigated the impact of dopant distribution and transport mechanisms in SOI-based Esaki diodes with different nanostructure widths. Significant differences were observed in electronic transport behavior, particularly in the negative differential conductance (NDC) region, influenced by the doping process, impurity and/or defect levels within the depletion layer. The device with a design width of 160 nm, although representing a set of devices with low yield, exhibited a strong dependence on V_{sub}, suggesting a dominant BTBT mechanism mediated by dopant (impurity) and defect levels. The device with design width of 7000 nm (microstructure) also exhibits features resembling Esaki diodes, even with a higher yield, but their dependence on V_{sub} is relatively weak.

Several factors may contribute to this discrepancy. Dopant and/or defect states may influence the tunneling current. The concentration gradient at the p–n junction may also introduce spatial variations in the potential gradient within the depletion region. Additionally, the non-uniform diffusion of dopants (impurities) during the doping process may lead to the formation of dopant clusters, implicitly affecting the device characteristics.

These findings highlight the need for further investigation into these factors in a comparative manner. A deeper understanding of how nanoscale structure width impacts the properties of Esaki diodes is essential for advancing device design towards functionalities in miniaturized electronic circuits.

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