Special Issue of the 8th International Advances in Applied Physics and Materials Science Congress (APMAS 2018)

Design of a Two Stage Operational Amplifier with Zero Compensation for Accurate Bandgap Reference Circuit

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Operational amplifiers have a wide range of applications in converters, comparators, voltage generators etc., and are designed flexibly based on the application. Bandgap reference circuit has a pivot role in mixed circuits. Requirement of constant voltage irrespective of process, voltage, and temperature variations are essential in analog and digital applications. Operational amplifier is the crucial entity in bandgap reference circuit for generating a constant reference voltage. Efficient and Low power operational amplifier is to be dealt with the bandgap reference circuit to yield high throughput. As operational amplifiers have many applications, a simple design with low power consumption, high gain, and reasonable unity gain band and phase margin are required for bandgap reference circuit design. In this paper, a 5 V two stage operational amplifier with zero compensation is designed for bandgap reference circuit applications. The two stage operational amplifier provided a gain of 73.52 dB, unity gain bandwidth of 3.89 MHz and phase margin of 63.23° with a power consumption of 0.9 mW. 0.18 μm CMOS technology SCL parameters used in the design.

DOI: 10.12693/APhysPolA.135.977
PACS/topics: Operational amplifier, gain margin, phase margin, zero compensation, low power, voltage references

1. Introduction

MOS Devices are becoming more efficient and useful in modern electronics, the integration of MOS per unit area is rapidly growing due to technology advancements [1]. Transistors are scaled down to micro or nanometer to increase the performance and minimize the area [2]. As the aspect ratio (W/L) changes, there is a tradeoff can be obtained among the speed, gain, and other parameters. Operational amplifier (op-amp) optimization process to model dc gain and higher unity gain band (UGB) frequency is described in [3, 4]. In this paper, a high gain two stage op-amp has been proposed, pole splitting miller compensation technique is used to achieve op-amp stability. The effect of variations in channel width and length on performance of two stage op-amp is discussed in [5]. This paper has five sections: two stage op-amp introduction is in Sect. 1, Sect. 2 describes the proposed two stage op-amp circuit, Sect. 3 describes op-amp design procedure, Section 4 describes the results and discussion and Conclusion are in Sect. 5.

2. Proposed op-amp circuit

A two stage op-amp circuit with bias and compensation is show in Fig. 1, where the transistors MND are the differential stage transistors, transistors MPL are the load transistors, and MNT is the tail current stage transistor, to provide gain, MPG and MNG transistors are connected as the gain stage. Transistor MNB is used to mirror current from the bias current stage to the tail current transistor MNT. Cc is the Miller compensation capacitor and CL is the load capacitance for the op-amp.

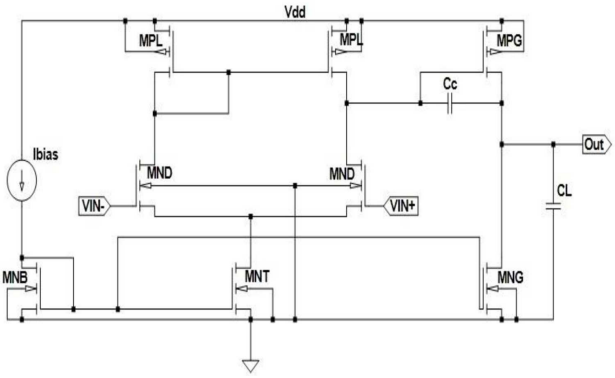

Fig. 1. A two stage op-amp with bias and miller compensation.

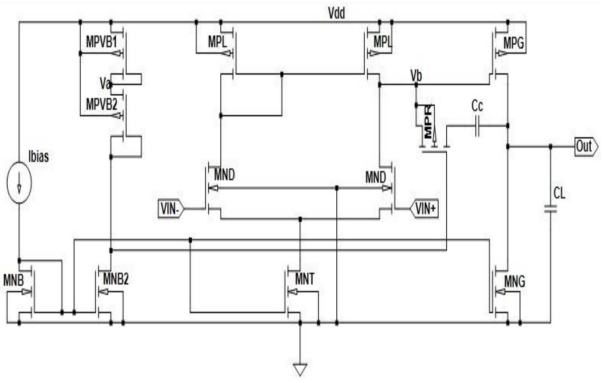

Fig. 2. A two stage op-amp with current bias and zero compensation.

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Proposed two Stage op-amp with Zero Compensation circuit is shown in the Fig. 2, in this, additional bias transistors (MPVB1, MPVB2 and MNB2) added in order to provide voltage bias and implement nulling resistor (MPR acts as a resistor for zero compensation in the circuit) at the output stage.

3. Design procedure

Op-amp design procedure contains several calculations and the relation between transistors with sizing procedure to meet desired desire specifications [6]. Here we discuss the designing of zero compensation transistors. The aspect ratio of transistor MPVB2 is essentially a free parameter and will be set equal to 1 and the current $I_{\mathrm{MPVB1}} = I_{\mathrm{MPVB2}} = I_{\mathrm{MNB2}}$ is half of the bias current

$$(W/L)_{\mathrm{MPVB1}} = \frac{I_{\mathrm{MPVB1}}}{I_{\mathrm{MPG}}} X (W/L)_{\mathrm{MPG}}$$

$$(W/L)_{\mathrm{MNB2}} = \frac{I_{\mathrm{MPVB}}}{I_{\mathrm{MNT}}} X (W/L)_{\mathrm{MNT}}$$

$$(W/L)_{\mathrm{MPR}} = \left(\frac{C_C}{C_L + C_C}\right) X \times \sqrt{\frac{(W/L)_{\mathrm{MPVB2}} (W/L)_{\mathrm{MPG}} I_{\mathrm{MPG}}}{I_{\mathrm{MPVB}}}}$$

4. Results and discussion

Cadence Virtuoso® analog design environment (ADE) is used to simulate the design at different process corners, at different voltages and at the different temperatures. With the requirement, tried to reduce the current in the high gain stage by considering the ratio of the current in that branch as a multiple of 5 and 2 instead of 10 are listed in the Table I, from this it is observed that the PM has reduced drastically when the current reduced to multiple of 2.

TABLE I
Simulation results for two stage op-amp.

	Gain [dB]	Phase [°]	UGB [MHz]	Settle [ns]	Slew [V/μs]
Initial design					
X10	74	79.98	3.98	190.6	20.04
Output current stage					
X2	74.075	35.92	4.344	195.4	17.51
X5	74.21	67.1	4.038	188.8	18.93

TABLE II
Simulation results for two stage op-amp before and after zero compensation.

	Gain [dB]	Phase [°]	UGB [MHz]
before zero compensation	74.075	35.92	4.344
after zero compensation	73.52	64.24	3.89

Zero compensation has done to increase phase margin. The results before zero compensation and after zero compensation are listed in the Table II.

Proposed zero compensated op-amp design has an open loop gain of 73.52 dB, 63.23° PM with a settling time of 194.4 ns. The slew rate of 17.51 V/μs is obtained with a load capacitance of 2 pF. The design total power consumption is 0.9 mW. For better understanding, Monte Carlo analysis has done through this the mean and standard deviation of the gain, Phase and UGB analyzed. From the Fig. 3a, it is observed the mean gain is 73.56 dB with a standard deviation (SD) of 1.376 dB. From the Fig. 3b, it is observed that the mean phase is 63.30° with SD of 935.154 °.

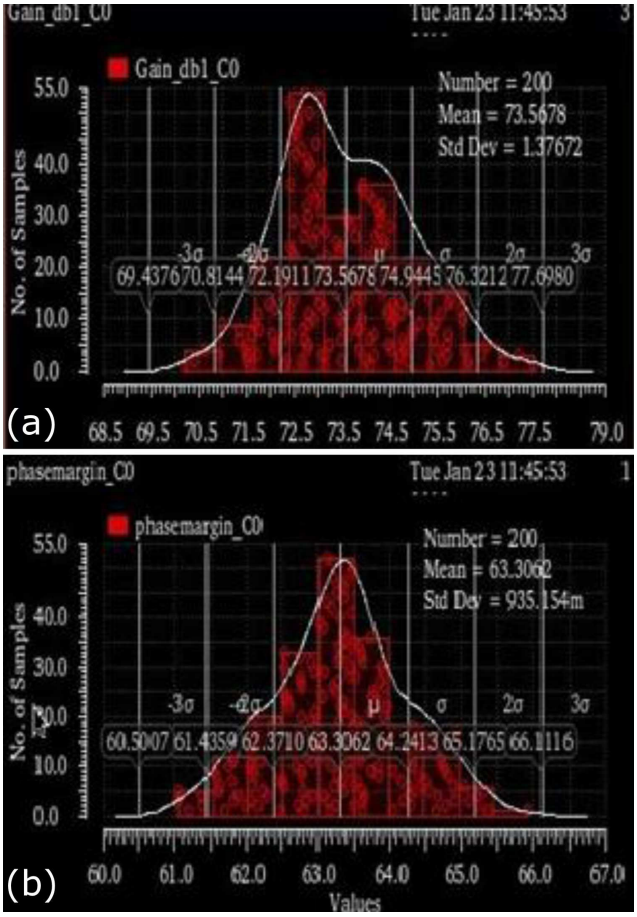

Fig. 3. Monte Carlo analysis: (a) gain plot and (b) phase plot.

5. Conclusion

A 5 V two stage op-amp circuit with zero compensation has been designed with 0.18 μm CMOS technology using SCL parameters. Zero compensation provided results of 73.52 dB gain, 3.89 MHz UGB and 63.23° PM even after reduced current in the high gain branch by the factor of 5 which leads to low power consumption. These are the better results when compared to the literature [5].

Acknowledgments

This research has been supported by SemiConductor Laboratory (SCL) Chandigarh, India. The author would like to be gratified for technical advice and support of SCL Scientists.

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