Investigation on the Effect of Delay Time during Pulse Chemical Etching of Porous Silicon Formation

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A set of porous silicon (PS) layers was produced by the pulse current (PC) etching technique using a solution of $HF:C_2H_6O$ in a composition ratio of 1:4 with delay time varying from 0 to 4 minutes. The set was compared with the one porous silicon sample that was etched by using the conventional direct current (DC) etching technique using the same ratio of solution. All the samples were etched at a current density of $J = 10$ mA/cm^2 for 30 minutes. During the PC etching process, the current was supplied through a pulse generator with 14 ms cycle time (T) which the on time (T_{on}) set to 10 ms and pause time (T_{off}) set to 4 ms respectively. An additional parameter called delay time (T_d) had been introduced during the etching process. Our results showed that the uniformity of pores produced was better with the application of the delay time. FESEM indicated that the variation of T_d affects the pore formation and pore size while EDX showed the composition of materials in PS. The HR-XRD analysis was also performed in order to investigate the structural characterization of produced PS.

1. Introduction

PS has become a promising material for the sensing application due to its unique properties such as high resistivity and wide energy bandgap that is suitable to be used in photo-detectors application [1]. The morphology of the pores can be influenced by several factors such as the applied current density, the composition of the electrolyte, the dopant level of the crystalline silicon substrate, not to mention the etching time [2]. PS was mostly produced using DC source etching of Si wafer in an (hydrofluoric) HF electrolyte [3–5]. However, there will be a formation of hydrogen bubbles on the surface of the pores during the etching process that will lead to the prevention of further silicon dissolution and which will result in shallow pores formation [6]. Amran et al. [7] further discovered that PS porosity and pore size can be improved by applying T_{off} during the etching process. Therefore the application of the PC can be used to obtain the T_{off} which can also help to reduce the hydrogen bubbles formation during the etching process. The reduction of the hydrogen bubbles formation during the etching process allows fresh HF species to get into the pores and react with the silicon wall while the rate of the etching process is maintained [8]. In this paper, a fixed cycle time of 14 ms has been applied for the pulse chemical etching technique with the introduction of delay time, while the other parameters remain the same as DC etching technique such

as the etching time and current density. Hence, the comparison of all samples will be observed and investigated in terms of its structural characterization.

2. Experimental procedure

All the samples have been cleaved into square shape with diamond tipped pen in 1 cm $\times$ 1 cm dimension. The square p-type (100) samples were cleaned by following the Radio Corporation of America (RCA) cleaning process where silicon wafers were dipped into heated chemical solution, 1:1:5 by volume of $H_2O_2:NH_4OH:H_2O$ for 10 minutes. Then, the samples were soaked in 1:50 of $HF:H_2O$ and then heated in 1:1:6 of $HCl:H_2O_2:H_2O$ for 10 more minutes. The anodization process has been used in the fabrication of PS with HF-based solution at room temperature under the illumination of incandescent lamp placed about 10 cm above the sample.

Figure 1 shows the schematic image of the anodization process setup. The backside of the Si wafer was directly contacted with the Al metal contact to enhance the uniformity of the anodic current flow during the etching process. The electrolyte consists of the mixture of HF with the concentration of 49% and ethanol 95% respectively, 1 : 4 by volume was poured into the single-tank cell. A platinum wire acting as cathode was dipped into the solution, while metal plate attached to the Si wafer acts as anode. PS samples have been fabricated under DC and PC etching techniques with the same current density of $J = 10$ mA/cm^2 for 30 minutes. As for the PC etching, the cycle time of 10 ms and pause time of 4 ms were supplied by the output signal from a pulse current generator. Both samples were then rinsed with deionized (DI)

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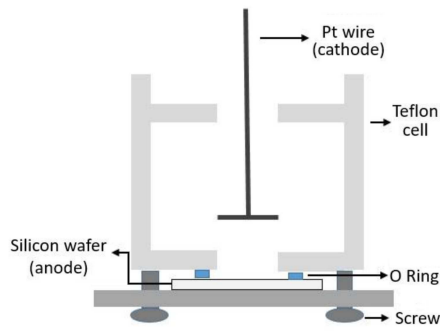[*]corresponding author; e-mail: hanieda@gmail.com

Fig. 1. Schematic image for the anodization process setup.

water and dried at ambient air at the end of the etching processes. FESEM, EDX, AFM, HR-XRD and Raman Spectroscopy have been used to characterize the samples. The Field Emission Scanning Microscopy (FESEM) and Energy Dispersive X-Ray (EDX) of both samples were taken using FEI Nanosem 450. FESEM analyzed the structure, pore size and surface morphology while EDX analyzed the composition of each elements of the fabricated PS samples. The surface morphology of the PS samples was then being observed by using the Atomic Force Microscope (AFM) where a damage on the sample surfaces can be prevented by applying tip scanning

using the "tapping" mode. The high resolution X-Ray diffraction (HR-XRD) spectrum is used to examine the degree of crystallinity from the fabricated PS samples. Finally, Raman spectra reveals the crystalline quality of the fabricated samples.

3. Results and discussion

Figure 2 shows the FESEM and EDX of PS samples that has been fabricated using DC and PC techniques with variations of time delay. The etching process on the nanometer scale produces different morphologies for each sample with different pore sizes. Porous sample which has been fabricated by DC technique, Sample A: DC in Fig. 2 shown non-homogeneous porous structure as a result of non-uniformly etched porous with pore size of 16.37 nm. Other three samples that have been fabricated by PC technique resulted in a homogeneous circular shape. However, by comparing those three samples, sample C: $T_d = 2$ with calculated average pore size 37.15 nm has the most homogeneous pores structure as compared to sample B: $T_d = 0$ with pore size 42.14 nm and D: $T_d = 4$ with pore size 51.03 nm. By referring to the EDX result, the silicon composition has increased after the introduction of 2 minute delay time with 98.04%.
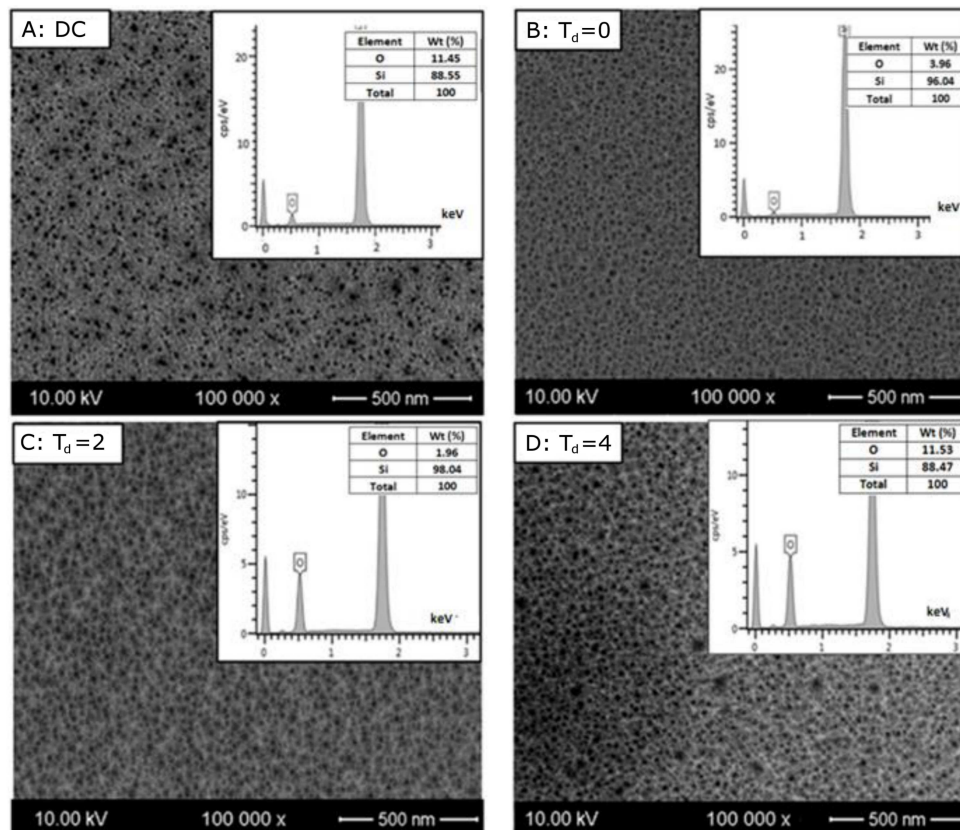

Fig. 2. FESEM images for PS samples: A — sample fabricated using DC technique, B — sample fabricated using PC technique with $T_d = 0$, C — sample fabricated using PC technique with $T_d = 2$ min, D — sample fabricated using PC technique with $T_d = 4$ min.
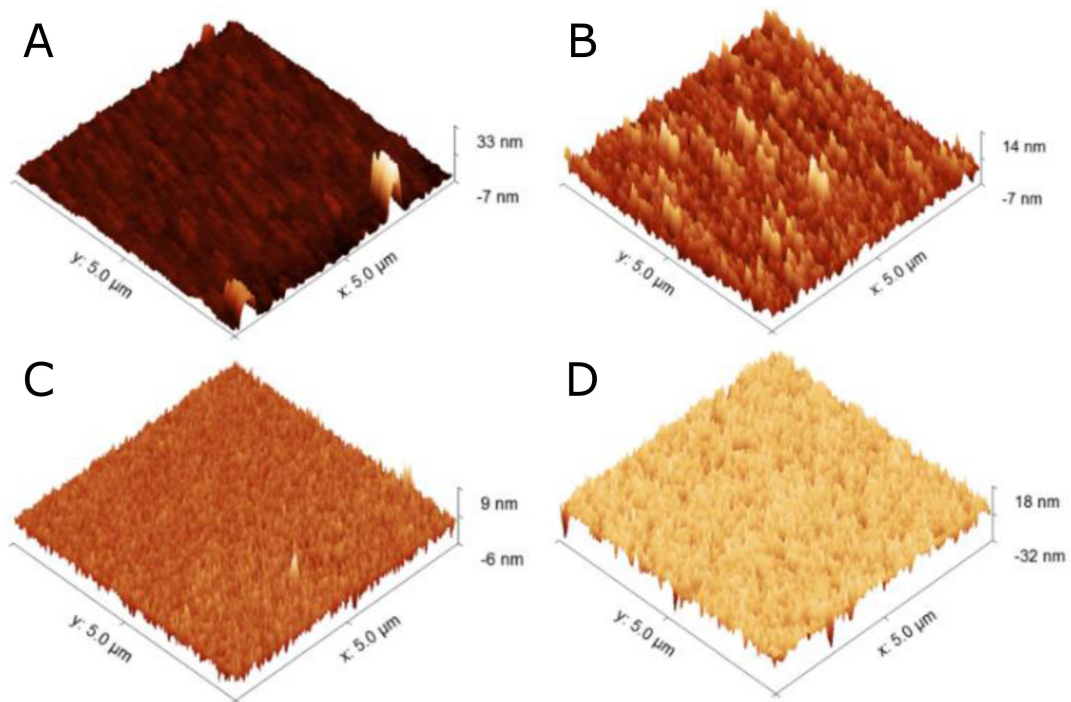
Fig. 3. 3-D AFM images for PS samples: A — sample fabricated using DC technique, RMS = 2.669 nm, B — sample fabricated using PC technique with $T_d = 0$, RMS = 2.225 nm, C — sample fabricated using PC technique with $T_d = 2$ min, RMS = 1.253 nm, D — sample fabricated using PC technique with $T_d = 4$ min, RMS = 4.634 nm.

However, the silicon element has been decreased showing that the increase in the delay time resulted in the decreasing percentage of the silicon element. Therefore, it can be concluded that the optimized value for delay time in order to get the maximum value of silicon element is 2 minutes based on the results shown in Fig. 2. Furthermore, the composition of oxide element decreases due to the reduction of the hydrogen bubbles formation which has stabilized the etching process, therefore minimal area of silicon wafer has been oxidized.

Figure 3 shows 3-D AFM images of all samples where the scanning area was 5μm $\times$ 5μm. It is clearly seen that there is a significant difference on the steepness of the Si columns for all samples. The surface of sample C: $T_d = 2$ shown more widely uniform and separated Si columns with steeper sidewalls than other three samples even though sample B: $T_d = 0$ and D: $T_d = 4$ were samples that produce through the pulsed electrochemical method as well. The root mean square (RMS) for A: DC sample is 2.669 nm and the value decrease when the PC etching method applied to the sample. Sample C: $T_d = 2$ exhibited lowest RMS value with 1.253 nm compared to other samples. However, due to the extended delay time causing sample D: $T_d = 4$ having highest RMS value of 4.643 nm.

Figure 4 shows the HR-XRD spectra of PS samples anodized with constant current, sample A: DC and pulsed current, sample B: $T_d = 0$, C: $T_d = 2$, and D: $T_d = 4$. The HR-XRD spectrum revealed two peaks at $2\theta = 69.125°$ and $2\theta = 69.325°$ which correspond to the crystal plane of (400) and (422) silicon cubic structures, respectively. The different etching techniques (DC and PC) and also different delay times introduced resulted in different morphologies and crystallinities.

The estimation of the average crystallite size has been calculated using Debye-Scherrer and were tabulated in Table I showing that the crystallite size has been decreased as the samples were etched using PC etching technique.
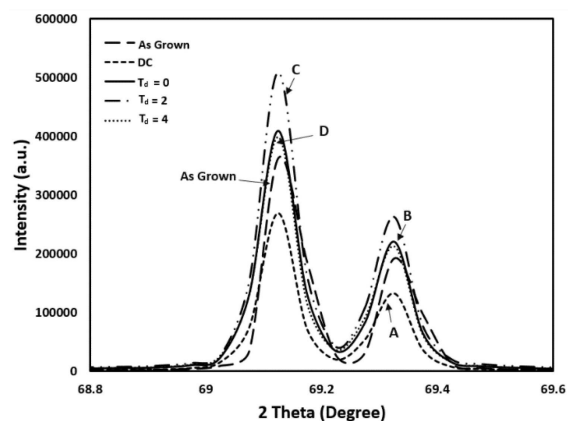

Fig. 4. The HR-XRD spectra for p-type (100) PS samples under different etching types: A — sample fabricated using DC technique, B — sample fabricated using PC technique with $T_d = 0$, C — sample fabricated using PC technique with $T_d = 2$ min, D — sample fabricated using PC technique with $T_d = 4$ min.

TABLE I

Peak position and FWHM for p-type (100) as grown, DC and PC samples with delay time.

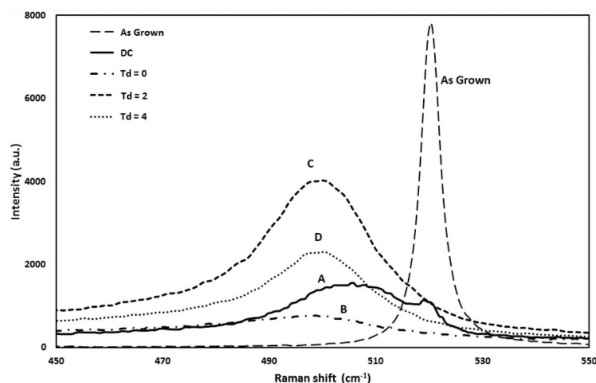| Samples	2θ [°]	FWHM [°]	Crystallite size [nm]
As Grown	69.13	0.11	77.276
A: DC	69.13	0.09	88.337
B: $T_d = 0$	69.12	0.12	66.246
C: $T_d = 2$	69.20	0.72	11.085
D: $T_d = 4$	69.20	0.59	13.522

Fig. 5. The Raman spectra for p-type (100) as grown and PS samples: A — sample fabricated using DC technique, B — sample fabricated using PC technique with $T_d = 0$, C — sample fabricated using PC technique with $T_d = 2$ min, D — sample fabricated using PC technique with $T_d = 4$ min.

TABLE II

Raman peak and peak shift for p-type (100) as grown, DC and PC samples with delay time.

Samples	Raman peak [cm^{-1}]	Peak shift [cm^{-1}]
as grown	520.33	–
A: DC	504.77	15.56
B: $T_d = 0$	497.79	22.54
C: $T_d = 2$	501.01	19.32
D: $T_d = 4$	500.47	19.86

Raman scattering spectroscopy is another way to estimate the nanocrystal characterization. Figure 5 shows the Raman spectra for all samples where sample C: $T_d = 2$ that exhibited a broader and asymmetrical Raman Spectrum with the highest intensity indicates better crystalline quality of the sample. Table II shows the Raman peak of each sample and the peak shift of as grown PS sample is included for reference.

4. Conclusion

In conclusion, the surface morphology indicated that the PS from the PC technique exhibited a more uniform structure and the highest composition of silicon element especially during 2 minutes time delay. Therefore it can be concluded that 2 minutes of delay time is the optimized value to be used in order to get the best structure of the PS sample. The periodical ON and OFF of the anodic current along with the introduction of time delay apparently initiates the recovery of HF concentration inside the pores and it can finally optimize the etching conditions. Atomic force microscopic observations of the surface reveal that the pulsed etching with appropriate delay time creates isolated Si columns with steeper sidewalls, which are in favor of achieving the quantum confinement effect.

Acknowledgments

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