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SOI FinFET Based 10T SRAM Cell Design against Short Channel Effects

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Continuous scaling of CMOS devices makes the density of Static Random Access memory (SRAM) array size increases. Maintaining high yield in SRAMs becomes more difficult at lower technology nodes, since they are unguarded to the process variations due to the large array size and cell miniaturization, this factor motivates towards the investigation of new techniques and technologies. FinFET technology is the promising technology with which all hurdles of CMOS technology can be overcome. In this paper, a novel 10T SRAM cell has been proposed, and is designed with both CMOS and FinFET technologies and finally the comparisons are made to know the better one. Synopsis TCAD and Cadence Virtuoso tools has been used to carry out SRAM designs.

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1. Background

Bulk CMOS scaling progress includes short channel effects (SCEs), sub-threshold leakage, gate dielectric leakage, and device-to-device variations. Reverse bias leakage, sub-threshold leakage, gate oxide tunneling, gate-induced drain leakage, and punch-through effects are some of effects [1]. The amounts of sub-threshold and gate oxide leakages are greater with the device scaling. Up to 65 nm, sub-threshold leakage dominates the gate leakage. Beyond 65 nm, the scenario is reversed. For a new technology, where 18% gate oxide thickness (t_{ox}) is reduced, the minimum thickness for reliable operation is 2 nm, but at 65 nm it is 1.4 nm. Hence the gate leakage is 1000 times more than the sub-threshold leakage [2]. To utilize the scaling benefits with minimum SCEs the device structures are continuously being tried to be modified. FinFET results due to the relentless increase in levels of integration. Based on the earlier depleted lean-channel transistor design [3], FinFET is built on an SOI substrate making it a non-planar and double gate device [4]. Double gate FINFETs overcomes scaling hurdles and its significant feature of Fin FETs is that the front and back gates can be made independent and biased to manage the current and threshold voltage. Typical FinFET design is presented in the papers [5–7].

2. Proposed 10T SRAM cell

Proposed 10T is shown in Fig. 1. Two leakage control transistors (PMOS and NMOS devices) are placed in each of the inverter in such a way that one of the transistors operates near its cut-off region. Drain nodes are connected together to form the output node of the inverter. Source nodes are connected to the pull-up and pull-down logic. By adding extra transistors the area increases, which can be overcome by sizing of the transistors while maintaining typical cell ratio and pull up ratios. This makes sure that one of the leakage controlling transistors is always near its cut-off region irrespective of the input. Use of leakage control transistors increases the path's resistance from the supply to ground. In CMOS technology, supply voltage scaling reduces the performance of 6T-SRAM cell severely [8]. To overcome these setbacks, Fin FET technology is alternative to the conventional technology.

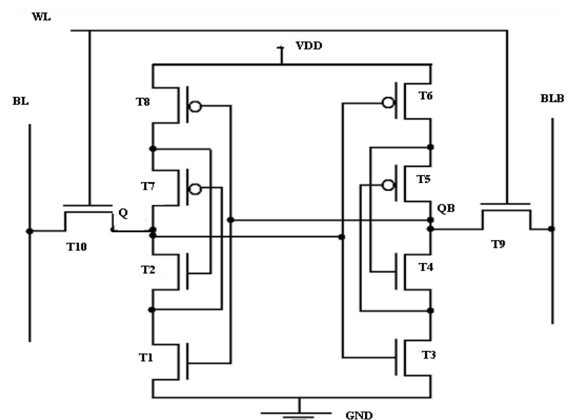

Fig. 1. Proposed 10T SRAM cell.

2.1. FIN FET technology SRAM

An enhanced read access time of 22 nm 6T SRAM cell can be achieved against the statistical variations in read and write cycles, corresponding to the supply voltage V_{dd} variations with a technique proposed in [8]. A number of designs were proposed in FinFET technology, but Tony Chopper methods are more popular for optimization

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various design parameters in different technologies [9]. A 45 nm FinFET based 6T SRAM cell is designed, and found that it has 69 pA leakage current, 7.581 nW leakage power, and 20.55 ns delay in write cycle. The circuit in [10] produces 53.90 pA leakage current, 1.709 μW leakage power, and 21.44 ns delay in read cycle. Proposed technique produced the results of 11.057 ps read access time and 12.233 ps write access time with $V_{dd} = 0.8$ V which is the nominal voltage for 22 nm FinFET and the power consumption of the FinFET 6T cell is 0.140 mW at 0.8 V.

3. Simulation results

Power graphs of proposed and modified10T FinFET SRAMs are shown in Figs. 2 and 3, respectively. Due to the increase in the capacitances, a spiky output is obtained while calculating the power, as shown in Fig. 2. Hence, the 10T SRAM circuit is modified as in Fig. 4.

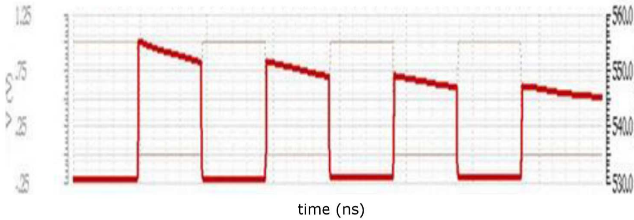

Fig. 2. Proposed 10T FinFET SRAM power graph.

From Fig. 3, it is observed that the capacitor is discharging at higher rate with the voltage applied, and also the graph has a linear slope, which indicates the amount of current flowing through the capacitor. As it has a constant slope, it implies that the current through the capacitor is also constant. Once again it proves that it is an advantage over the MOSFET as it does not violate absolute maximum current rating and the reliability increases.

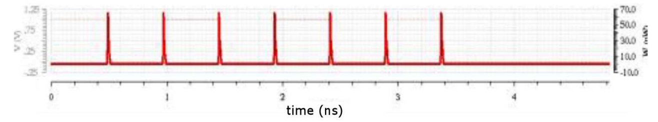

Fig. 3. Modified 10T FinFET SRAM power graph.

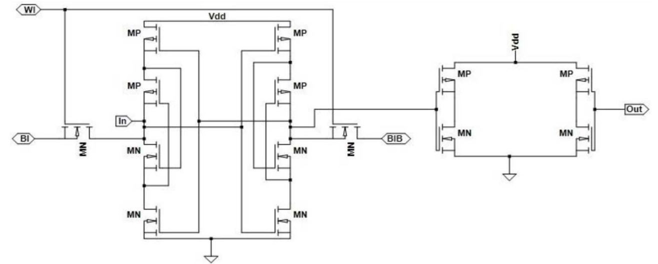

Fig. 4. Proposed modified 10T SRAM circuit.

4. Results and analysis

Power and stability of the 6T and 10T SRAM cells are discussed. From Table I, it is observed that the FinFETs are stronger than CMOS and the proposed design is more stable.

Peak and average powers of 6T and 10T SRAMs for both FinFET and CMOS technologies are calculated and given in Table II. From the results, it is observed that the FinFET technology shows better performance compared to CMOS technology.

TABLE I

Stability analysis of CMOS and FinFET technologies

Supply voltage V_{dd} [V]	45 nm CMOS			14 nm Fin-FET		
	6T SRAM[11]	10T SRAM	Proposed 10T SRAM	6T SRAM	10T SRAM	Proposed 10T SRAM
0.85	stable	stable	more stable	stable	stable	more stable
0.70	less stable	stable	stable	stable	stable	more stable
0.65	unstable	stable	stable	less stable	stable	stable
0.60	more stable	less stable	stable	unstable	less stable	stable

TABLE II

Technology power comparison table

Technology	Peak power		Average power	
	45 nm (CMOS)	14 nm (Fin FET)	45 nm (CMOS)	14 nm (Fin FET)
6T SRAM	2.58 mW	0.091 mW	2.602 mW	0.089 mW
10T SRAM	62.767 μW	40.65 μW	0.043 μW	0.018 μW
Proposed 10T SRAM	42.23 μW	27.41 μW	0.0211 μW	0.005 μW
Modified proposed 10T	44.11 μW	29.03 μW	0.0317 μW	0.0141 μW

5. Conclusions

In this paper, a novel 10T SRAM cell has designed in both CMOS and FinFET technologies, and the proposed design shows better results in both the technologies in the view of stability and power consumption when compared with the cell designs in the literature. A model FinFET is developed using synopsis TCAD tool. From results, it is observed that the CMOS designs failed especially when the design is carried out at lower technology nodes due to the SCEs, and are more prone in MOS-

FETs with the device scaling. To grab the advantage of technology down scaling, FinFET technology would be preferred, since FinFETs minimizes most of the SCEs.

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