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Investigation on the Effect of Direct Current and Integrated Pulsed Electrochemical Etching of *n*-Type (100) Silicon

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This paper investigates the effects of different etching techniques between direct current electrochemical etching (DCPEC) and integrated pulsed electrochemical etching (iPEC) on the structural and optical characteristics of porous silicon formation. The *n*-type Si (100) was fabricated using both techniques in an electrolyte that consists of aqueous hydrofluoric acid (HF) and ethanol (C_2H_5OH) with a ratio of 1:4. An additional pulse cycle of 14 ms with $T_{\rm on} = 10$ ms and $T_{\rm off} = 4$ ms was supplied for iPEC porous silicon sample. The finding from both samples showed that the pore formation was affected by the etching techniques used. The porous silicon etched by the DCPEC technique produced a square-like pore with a porosity of 40% while the iPEC technique formed a mix of square and crossed shape pore with a porosity of 52%. From atomic force microscopy, the sample prepared by DCPEC was identified to have a deeper pore that causes larger crystallite size and better intensity in the Raman and photoluminescence spectra. On the other hand, the iPEC technique produced a higher and larger value of surface porosity and pore diameter but it has a shallower pore. The photoluminescence peak corresponding to red emission (*S*-band) is observed at 642 and 637 nm for DCPEC and iPEC samples, respectively. This is due to the nanoscaled size of silicon through the quantum confinement effect that was estimated to be around 7.9 nm and 7.8 nm for DCPEC and iPEC samples, respectively, determined from the quantized state effective mass theory.

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PACS/topics: porous silicon, electrochemical etching, pulsed electrochemical, surface morphology, optical characteristics

1. Introduction

Silicon (Si) based devices have been further developed and have paved the way in the semiconductors industry. However, Si has been claimed to be unstable for optoelectronics applications due to its indirect bandgap, which may reduce its efficiency as a light emitter [1]. Therefore, the porous structure on the Si material was introduced to improve the light-emission properties of Si as discovered in [1, 2]. The formation of the porous structure on the Si surface provides several advantages. For example, the porous structure produces greater surface area than bulk Si, as it allows more optical activities to occur at the Si surface [2]. On top of that, by applying this structure on a Si surface, the quantum confinement effect is predicted to bring about an increased modification in the density of electrons, phonons, and a carrier of electron–hole pair recombination [1]. Hence, porous Si has widely been used in many applications.

There were two techniques that have been used to create a porous structure on a semiconductor surface, namely, dry and wet etching. However, the dry etching methods could cause surface damage because this type of etching involves a very high kinetic energy atom being bombarded to the material surface. On the other hand, in wet etching, liquid chemicals or etchants are used to remove the exposed materials. Electrochemical etching is a common method of wet etching that can create pores on silicon through the use of the anodization cell. The electrochemical etching technique is of low cost and easy to implement, has a high etching rate as well as good selectivity for most materials compared to dry etching [3, 4]. Therefore, wet etching is more preferable than dry etching to fabricate the porous structure on the Si material.

Commonly, the wet etching technique use DCPEC in HF acid based electrolytes. However recently, there are works such as [1, 2, 5, 6] that implement the iPEC technique. The idea to integrate the iPEC technique is to rest and pause the current temporarily. By doing so, it allows the sample to eject the H_2 bubbles and at the same time allow fresh HF to penetrate into the pores and react with the substrate, which can enhance the etching process at

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a significant rate [1]. Therefore, the aim of this work is to investigate the effect of DCPEC and iPEC etching techniques on the structural and optical characteristics of the porous Si.

2. Experimental details

The porous Si samples in this work were fabricated by using both the etching techniques of DCPEC and iPEC. The work started with the 2 inch diameter of Si n-type (100) wafer being diced into a smaller dimension of approximately 1 cm × 1 cm sample prior to be fitted in the Teflon cell. Before undergoing the etching process, the Si wafer sample was needed to be cleaned by following the Radio Corporation of America (RCA) cleaning procedure. The Si sample was installed through the O-ring so that only the front surface was being exposed to the electrolyte solution. Then, the metal plate was being clamped tightly by using two screws to ensure that there is no leakage of the electrolyte during the etching process. In both techniques, the porous structure on the Si sample was fabricated with a current density of 20 mA/cm^2 for 20 min in the electrolyte that consists of aqueous HF and ethanol (C_2H_5OH) with a ratio of 1:4 under the illumination of incandescent lamp. An additional pulse cycle of 14 ms with T_{on} of 10 ms and T_{off} of 4 ms was supplied for the iPEC porous silicon sample. After the etching process, all the samples were rinsed with deionized (DI) water. The surface morphology and topography of the porous Si were characterized by the field emission scanning electron microscopy (FESEM) (Model: JEOL JSM 7401F) and atomic force microscopy (AFM) (Model: Dimension EDGE, Bruker). The NanoScope Analysis software was used to analyse the surface roughness and the estimated pore depth of the samples with scan area of 5 × 5 μm^2. Both of the samples also undergo the energy-dispersive X-ray spectroscopy (EDX) to determine the composition of each material existing on the porous Si surface. High resolution X-ray diffraction (HRXRD) (Model: PANalytical X'pert Pro MRD) was used to assess the crystalline quality of the samples. To study the optical characteristic of the sample, the Raman (Model: Renishaw InVia Qontor) and photoluminescence (PL) (Model: Edinburgh Instrument, FLS920) spectra were carried out. A He–Ne laser (λ = 633 nm) and Xenon lamp (λ = 300 nm) were used as an excitation source for Raman and PL, respectively.

3. Results and discussion

Figure 1 shows the top view image from the FESEM and EDX analyses of porous Si samples subjected to different etching techniques. Figure 1a shows the surface morphology of the porous Si etched by using the DCPEC technique. It can be seen that there are non-uniform square-like shape pores on the sample surface with an average pore diameter and estimated porosity of ≈ 0.46 μm, and 40%, respectively, as measured using Image J. Similar square pore morphology has been observed in [7, 8] which indicates that Si n(100) by using DCPEC techniques resulted in square shape pore. On the other hand, the porous Si sample etched using iPEC technique as shown in Fig. 1b formed a mix of square and crossed shape pores with an estimated porosity of 52%. The average square pore diameter was ≈ 0.72 μm while the crossed intersecting pore diameter was ≈ 1.74 μm. There is similar morphology noticed as in [1, 2] using the same etching technique.

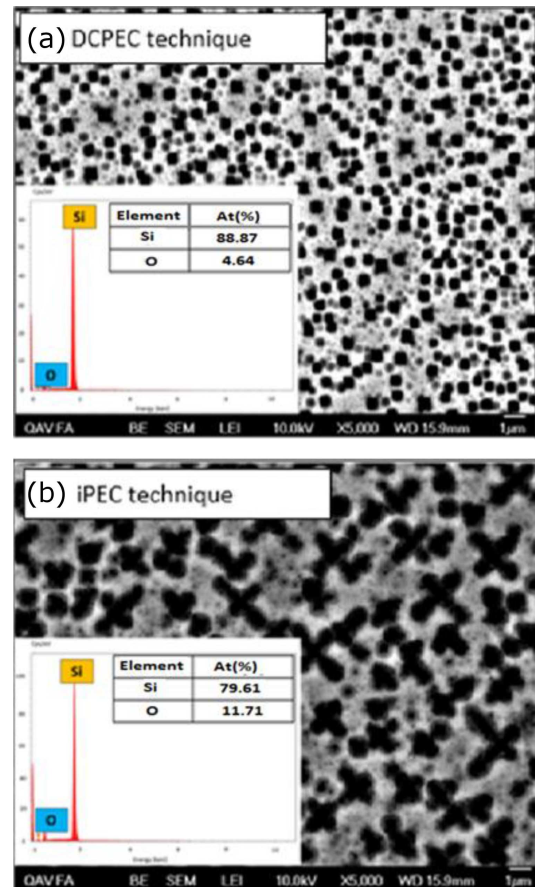

Fig. 1. SEM images and EDX of porous silicon samples fabricated using (a) DCPEC and (b) iPEC technique.

By comparing the surface porous formation from both samples, the iPEC sample has a greater porosity and pore diameter. The most acceptable reason for the difference in the surface pore formation is the presence of T_{off} in the iPEC sample. T_{off} allows the sample to eject the H_2 bubbles and at the same time allow fresh HF to react with the sample surface. This eventually enhances the etching rate and as result, creates a higher porosity at the sample surface, as reported in [2]. Furthermore, Amran et al. [1] also stated that during T_{off}, the samples tend to remove the oxide at the sample surface, indicating the barrier layer thinning and hence, allowing higher current to operate at the next T_{on}. The EDX result from

Fig. 1 confirmed only the presence of significant silicon (Si) and lower oxygen (O) content at the surface for both samples. This indicates that there are no traces of other elements in the EDX spectrum. The iPEC sample has less value of silicon atom (79.61%) compared to DCPEC sample (88.87%) and this could be due to having larger porous structures (more Si has been etched) and smaller crystallite size of silicon on the surface.

The 3D AFM images of the sample fabricated using DCPEC and iPEC techniques were shown in Fig. 2. The DCPEC sample has a larger value of surface roughness with the RMS value of 26.8 nm compared to the iPEC sample with the RMS value of 10.9 nm. This indicates that the DCPEC sample has a rougher surface than the iPEC sample, explaining that it has more pronounced pores. Meanwhile, in terms of the estimated average pore depth, as calculated from the cross-section line scan as shown in Fig. 2a and b, the sample etched by the DCPEC techniques was deeper than the sample prepared by the iPEC technique with values of ≈ 105 nm and ≈ 36 nm for DCPEC and iPEC samples, respectively. By taking into account both results from the FESEM (Fig. 1) and AFM (Fig. 2) analyses, it can be concluded that the sample etched by the DCPEC technique formed a smaller and deeper pore while by using the iPEC technique, the pore formed is shallower but bigger at the sample surface. The significant difference on the pore formation between DCPEC and iPEC techniques may be explained by the difference in the etching mechanism. The formation of the pore was illustrated in Fig. 3a for sample etched by using DCPEC technique and Fig. 3b for sample fabricated by iPEC technique. As for the DCPEC technique, the current flow went without any interruption for 20 min during the etching process. This allowed the interaction of an electrolyte toward the sample occurring gradually, resulting in deeper pores. However, in the iPEC technique, there is an interruption of the current flow during $T_{\rm off}$. On the next $T_{\rm on}$, an electrolyte–Si interaction tends to create new pores at the sample surface rather than continuing with the previous pores formed. This explained why the sample fabricated by the iPEC technique produced a mix of larger square and crossed shaped pores at the sample surface that were shallow in depth.

Therefore, the setting of $T_{\rm on}$ and $T_{\rm off}$ must be in an appropriate ratio for a better formation of the porous structure as suggested in [1]. On the other hand, Naderi et al. claimed that the application of delay time in the iPEC technique can enhance the etching rate and may result in a uniform and deeper pore as it combined electroless and electrochemical etching [5, 6] for the iPEC etching technique. Figure 4 shows the 2Θ-scan patterns of the sample etched due to different etching techniques. It reveals that there are two peaks that exist for both samples at $2\theta = 69.13°$ and $2\theta = 69.33°$, corresponding to (400) and (422) cubic plane, respectively. However, the peaks at $2\theta = 69.13°$ are more prominent. Similar patterns are found in [1, 9], demonstrating its single crystalline (c-Si) nature.

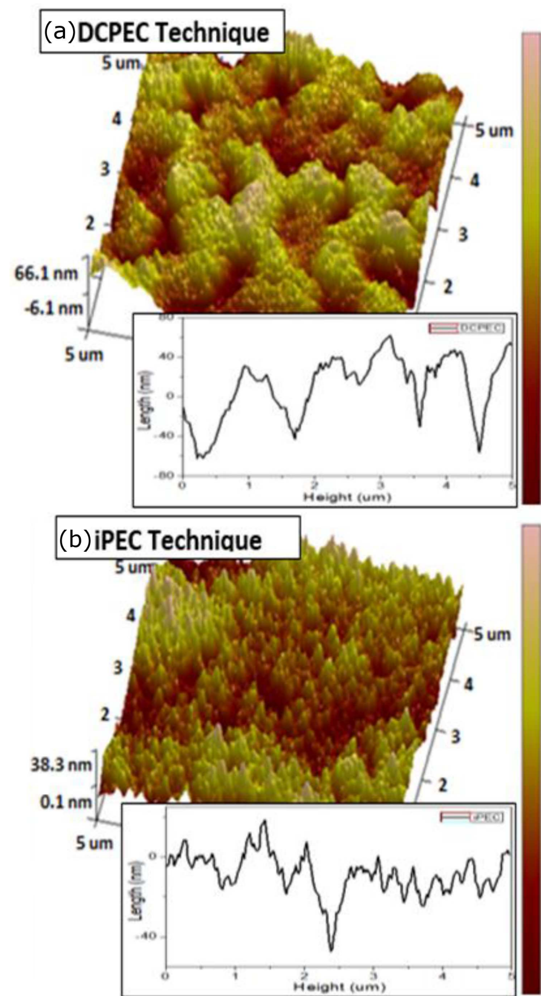

Fig. 2. 3D images and cross-section line scan of porous silicon samples fabricated by using (a) DCPEC and (b) iPEC technique.

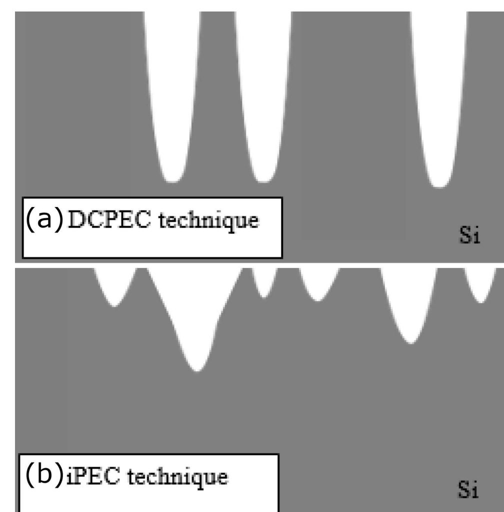

Fig. 3. Illustration of pore formation by using (a) DCPEC and (b) iPEC technique.

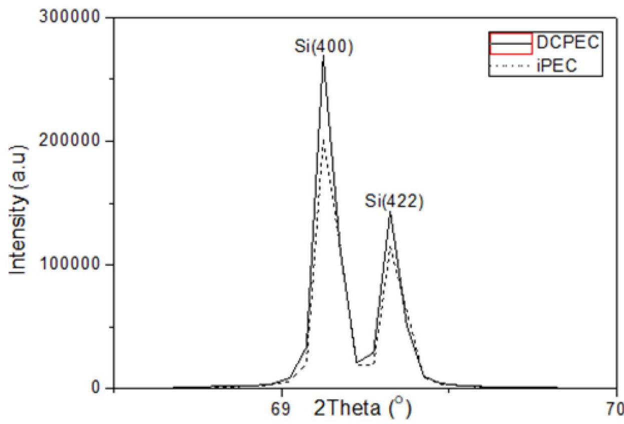

Fig. 4. 2Θ-scan patterns of sample etched by DCPEC and iPEC technique.

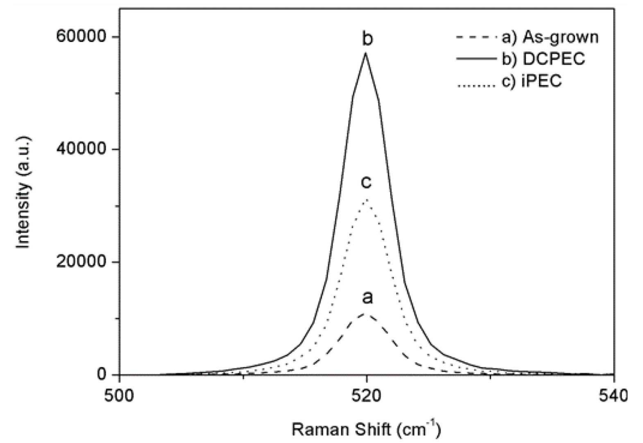

Fig. 5. Raman spectra of (a) non-porous and porous silicon etched by (b) DCPEC and (c) iPEC technique.

It can be seen that both of the samples etched by DCPEC and iPEC techniques have the same peak position. However, the porous silicon sample etched by the DCPEC technique has a higher peak of intensity compared to the iPEC sample. As for the full width half maximum (FWHM), both of the samples have a slight difference in value that is 0.10° and 0.11° for DCPEC and iPEC samples, respectively. The lower value of FWHM indicates the better crystallinity of the sample [10]. The Debye–Scherrer equation as in [11] was used to calculate the crystallite size of the samples and it reveals that there is not much difference between the samples etched by DCPEC and iPEC samples, 1.01 μm and 0.92 μm, respectively. However, the DCPEC sample shows a larger value of crystallite size as subjected to its smaller FWHM value.

Figure 5 shows the Raman spectra of the porous silicon sample etched by using different etching techniques. The spectrum corresponding to the non-porous Si as-grown is also plotted as reference. All samples' peak positions lie at the Raman shift of 519.9 cm^{-1} explaining that there is no difference for both samples in terms of the peak position, corresponding to the as-grown sample. Similar peak position was also observed and reported by [5]. These results reveal that no peak shift occurs and the stress relaxation is not related to the pore size as also claimed in [10]. As there is no broadening that occurs, the FWHM value (7.37 cm^{-1}) is similar for all samples. Furthermore, the DCPEC sample shows higher intensity in the Raman spectra compared to as grown and iPEC sample. This may be correlated with the pore depth of the sample as the sample etched by the DCPEC technique has a deeper pore.

The PL spectrum at room temperature for the porous silicon prepared by DCPEC and iPEC techniques is shown in Fig. 6. Both samples show a red emission with slight difference in the peak wavelength. The DCPEC sample has a peak wavelength at 642 nm (1.93 eV) while the sample produced by using the iPEC etching technique has a peak wavelength of 637 nm (1.95 eV). The *S*-band PL emission as observed in both samples indicates the quantum confinement of electrons in the nano-sized particles in the porous silicon [12]. In addition, as claimed in [13], the increase in the PL intensity is attributed to the total volume of the oriented nanocrystalline on the porous silicon surface, indicating that both etching techniques produced a nanostructure pore on the silicon sample. Therefore, to verify the nanostructures pore size for both samples, the effective mass theory as in [12] was used. From the calculation, it can be concluded that the observed PL peak at 642 nm and 637 nm is reasoned by the Si nanocrystallites with the diameter of about 7.9 nm and 7.8 nm for DCPEC and iPEC samples, respectively.

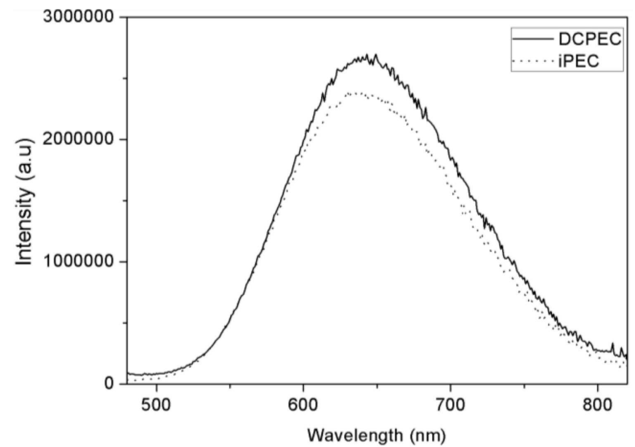

Fig. 6. PL spectra of porous silicon etched by DCPEC and iPEC etching technique.

4. Conclusions

The porous silicon was successfully fabricated using both etching techniques of DCPEC and iPEC techniques. From the results, both of the etching techniques produced different shapes and sizes of porous structure. The porous silicon etched by the DCPEC technique produced

a square-like pore while the iPEC technique formed a mix of square and crossed shape pores. The sample prepared by the DCPEC technique produces a nanostructure and deeper pore, resulting in larger crystallite size and better intensity in the Raman and PL spectra. On the other hand, the proposed iPEC technique contributed to a higher and larger value of surface porosity and pore diameter but it lacks the pore depth causing it to have a smaller intensity compared with the DCPEC sample on XRD, the Raman spectra, and also PL spectrum. Similar structure had been found in previous study conducted in [7, 8] for DCPEC etching technique and [1, 2] for iPEC etching technique. Hence, the etching technique plays an important role in order to form either small diameter with deeper pore (DCPEC technique) or large diameter with shallower pore (iPEC technique), depending on the device application. However, as suggested in [1, 2], the application of the time delay and appropriate ratio of T_{on} and T_{off}, the etching rate for the iPEC technique can be enhanced, resulting in deeper pore structure.

Acknowledgments

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