Proceedings of the International Conference on Oxide Materials for Electronic Engineering, May 29–June 2, 2017, Lviv

# Comparison of Electrical Performances of Power Electronics Switches and an Effective Switch Selection Algorithm

# H. Zenk\*

Giresun University, Engineering Faculty, Department of Electrics and Electronics, 28200 Giresun, Turkey

Electronics switches commonly used in power electronics circuits are the part of the electronics system depending on energy efficiency, circuit topology, switching matrix design, interaction with filter elements, and many other parameters. For the first new switch design prototype to identify of electrical efficiency of the semiconductor switch working with a system, it is very important that estimation of the variables saves time, labor, and economical resources. In this study, the new algorithm is proposed and applied to circuit estimate efficiency of power electronics switches. The current–voltage–power capacities, switching rate, power losses, physical dimensions, heating levels of power electronics switches used in the circuit are investigated and algorithmically estimated according to the result of experimental performance switches.

DOI: 10.12693/APhysPolA.133.897

PACS/topics: power electronics switches (PES), switch selection algorithm (SSA), IGBT, MOSFET, BJT, diode

# 1. Introduction

Some electrical conversions are needed to enable the generated electrical energy to be used by all devices [1]. The devices that make these transformations can be defined as power electronics switches (PES). The basic circuit of the modern power electronics keys is the switching matrix shown in Fig. 1, which typically can operate at frequencies above kHz. This circuit does not include energy storage units. However, in order to soften the current and voltage waves in the pulsating state of the input and output of the matrix, passive flicker filters are placed on the input and output sides of the circuit. As known, the most common method in switching is pulse width modulation (PWM) [2]. In this method, the magnitude of voltage/current pulses is constant and the frequency and width of the current/voltage is checked.

The higher the switching frequency, the smaller the filter size. But the switching losses are also increased. For this reason, the switching frequency of large power systems is reduced (100 kHz at 1 kW, 10 kHz at 100 kW, less than 1 kHz at 1 MW). In power supply design, parameters are very important, such as small size, low cost, and high energy conversion efficiency [3].

The most important factors determining the feasibility and commercial success of a product that is planned to be developed are parameters such as energy conversion efficiency, energy consumption, key life, size and cost of the PES to be used. The efficiency in PES depends on the switching and control methods and parameters as well as the basic power circuit elements. Taking good design decisions in pre-production computer environment save time, labor, infrastructure and material resources. Simple and accurate modeling of the switches and passive circuit elements for the practical and precise estimation of efficiency and switching functions must be defined. Thus efficiency calculation and improvement can be realized by considering various circuit topologies, circuit elements, switch types and switching methods. There is an algorithmic method requirement for key selection from a general point of view. An algorithmic efficiency estimation method is proposed in this study.

The main factors affecting the efficiency of PEScontaining systems are passive element losses and semiconductor losses (Fig. 1). Passive element losses in PEScontaining systems can be explained by calculation of some approximate formulae of capacitor and inductor effects. On the other hand, semiconductor losses are switching and transmission losses, computation with sufficient accuracy has difficulties in modelling complexity and parameter multiplicity. However, accurate calculation of semiconductor losses is of great benefit. The selection and evaluation of the topology of PES-containing systems, the selection of semiconductor switches and switching frequencies, and the design of the drive circuit, thermal design, make the parameters much easier. This study presents an algorithmic calculation method that calculates the semiconductor losses based on datasheet information.

Semiconductor losses mainly consist of switching, conduction and holding losses. Holding losses therefrom are negligible ( $\ll 1\%$ ) since in most applications they constitute only a fraction of the total loss of the semiconductor. Thus, switching and transmission losses constitute almost all of the semiconductor losses. The main factors affecting switching and transmission losses of PES-containing converters are the individual current/voltage and the duty cycle of semiconductors. In this study, instantaneous conduction losses of four basic semiconductor MOSFETs, IGBT, BJT and diodes, and the switching power per switching event and the current-voltage stresses of these switches are investigated. The mean

<sup>\*</sup>e-mail: hilmi.zenk@giresun.edu.tr



Fig. 1. Basic structure of power electron cycle system and demonstration of semiconductor losses.

power loss over the baseline period, which is topology dependent, is modeled by these parameters.

### 2. Semiconductor loss

The current, voltage, and frequency parameters of the circuit containing the semiconductor switches are selected according to the basic design magnitudes. While MOSFETs are preferred as low-voltage, high-frequency active switches, high-voltage and low-frequency IGBTs are at the forefront. The RCE-on, VCE-on, and switching energy curves are taken into account when choosing IGBTs and BJTs, while RDS-on value and door load curves are important for MOSFET selection for efficiency optimization. The addition of reverse recovery current characteristics to the RD-on and VD-on values of the diodes is important for high efficiency.

# 2.1. IGBT losses

The test circuit in Fig. 2 belongs to an IGBT shown with its parasitic elements [4]. Immediate conduction losses of IGBTs with minority carriers are dependent on the transmission resistance  $(R_{CE-ON})$  and constant



Fig. 2. IGBT switching test circuit.



Fig. 3. IGBT  $i_C - V_{CE}$  chart.

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Fig. 4.  $I_c$ ,  $R_G$  and  $T_c$  graph of IGBT switching power.

voltage drop  $(V_{CE-ON})$  values as shown in Eq. (1) [5, 6].  $V_{CE-ON}$  can be obtained directly as shown in Fig. 3. The  $R_{CE-ON}$  value is calculated from the slope as given in Eq. (2) according to the  $V_{GE}$  value

$$P_{IGBT-C}(t) = i_C(t) v_{CE-ON} + i_C^2(t) R_{CE-ON}, \quad (1)$$

$$R_{CE-ON} = \frac{\Delta v_{IGBT}}{\Delta i_{IGBT}}.$$
(2)

The switching powers of IGBTs in conduction and cut-off conditions are different from MOSFETs,  $i_C$ ,  $T_j$ , and varying  $R_G$  values are usually obtained from IGBT datashet data as shown in Fig. 4. From these graphs, it is necessary to make the polynomial convergence to the  $i_C - E_{on}$ and  $i_C - E_{off}$  curves second-degree and to reflect the other curves as a scale factor to the energy loss polynomial by proportioning to the given test operating conditions.

#### 2.2. MOSFET losses

The test circuit used for a typical MOSFET is shown in Fig. 5. Immediate conduction losses of MOSFETs with majority carrier semiconductors are the resistive losses defined in Eq. (3) in which reveals that MOSFET resistor  $R_{DS-on}$  is the function of  $i_D$  MOSFET current,  $V_{GS}$  gate voltage and  $T_i$  junction temperature.

These correlations are usually given in the MOSFET datasets and should be used in conjunction with operating condition parameters for a more accurate instantaneous power dissipation approach

 $P_{M-C}(t) = i_D^2(t) R_{DS-ON}(i_D(t) V_{GS}T_j).$  (3) Switching losses of MOSFETs are calculated by energy loss per switching. This energy is calculated based on the current and voltage rise and fall times [7]. The rise/fall times are calculated more accurately by the  $Q_g - V_{GS}$ curves as in [8], instead of the switch-on parasitic capacitors changing by VGS gate voltage. Figure 6 shows the  $Q_g - V_{GS}$  characteristics for the MOSFET [9]. Figure 7 shows the typical conduction and cut-through terminal currents/voltages of the MOSFETs. Taking this graph, the switching rise/fall times can be calculated as given in Eq. (4), assuming constant  $i_G$  for current rise/fall times and using  $R_{G-on}$  and  $R_{G-off}$  resistors.

$$E_{M-SW-r-f} = \frac{1}{2} V_{block} I_0(t_{r-i} + t_{r-v} + t_{f-i} + t_{f-v}), \quad (4)$$

$$E_{M-SW-COSS} = \frac{1}{2} C_{OSS} V_{block}^2, \tag{5}$$

$$E_{M-SW-Q-rr} = V_{block} Q_{rr}, \tag{6}$$

$$E_{M-SW} = E_{M-SW-r-f} + E_{M-SW-COSS} + E_{M-SW-Q-rr}.$$
(7)



Fig. 5. MOSFET switching test circuit.

# 2.3. Diode losses

Immediate conduction losses of the diodes are calculated by Eq. (8). Here  $V_{D-ON}$  and  $R_{D-ON}$  are obtained in a similar manner to the  $V_{CE-ON}$  and  $R_{CE-ON}$  parameters in the IGBT [7]. The switching energy losses of the diodes occur during the current interruption due to the reverse recovery current. In Fig. 8, the reverse recovery of the diode is indicated by the terminal current and voltage at the cutting line. The switching energies associated with the inverse restraint load, which is dependent on the operating conditions of the diodes, and the tension in the legs are given in Eq. (9). The reverse load on



Fig. 6. An example of MOSFET  $Q_g - V_{GS}$  characteristic.



Fig. 7. The switching characteristic of the MOSFETs is (A) the switch voltage and current, (B) gate voltage, (C) gate current.

the diode cutting line changes with parameters such as the forward current, the deceleration rate of the current cut (derivative) and the temperature. The relationship between the descent rate of the current cut from these parameters is given in Fig. 9. The addition of these parameters to the account polynomial convergence and the scale factors. With the progress of power semiconductor technology, the reverse current problem in the diodes and therefore the reverse load and the losses due to it have been reduced considerably.

$$P_{D-C}(t) = i_F(t) V_{D-ON} + i_F^2(t) R_{DS-ON}, \qquad (8)$$

$$E_{D-SW} = \frac{V_{D-block}Q_{rr}(I_{F-ON}, dI_F/dt)}{4}.$$
(9)

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Fig. 8. Terminal currents and voltages that indicate the reverse recovery phenomenon in the instantaneous part of a power diode.



Fig. 9. Dependence graph of the reverse recovery charge for the diode on the rate of decrease of the diode current.

# 3. Modeling system losses

It is necessary to calculate the switching loss  $(T_s)$  values of the instantaneous conduction losses of the semiconductors and the switching losses of the conduction/cutting crossing. Equations (10) and (11) are given for a period of transmission and switching losses. In Fig. 10, this process is visualized for a switch. In Fig. 10, k is the switching index. Equations (10) and (11), where the highest value  $(k_{max})$  is the exact value of the ratio of a fundamental period to the switching period, are the following:

$$P_{C-Ts}[k] = \frac{1}{T_s} \int_{kT_s}^{(k+1)T_s} P_C(t) dt, \qquad (10)$$

$$P_{S-Ts}[k] = \frac{1}{T_s} \sum_{k=1}^{\infty} E_{SW} \|_{kT_s}^{(k+1)T_s}.$$
(11)

The current signal shown in Fig. 10a flows when switch conduction passes. When switch is in cut position (off position), a voltage is generated between its terminals  $(V_{block})$ . This current and voltage is the current/voltage across the semiconductors  $T_s$  difficulty is. In Fig. 10c, the instantaneous switching losses on this switch are shown symbolically. These instantaneous switching losses are defined as energy and divided by  $T_s$  to obtain the average lost switching power over a switching period as in Fig. 10d. In Fig. 10e, the transmission losses of this switch can be calculated as in Fig. 10f, taking a switching period average.



Fig. 10. Indication of the calculation of transmission and switching losses for a switch with sudden switching.

In a circuit with a fixed switching frequency, given in (10) and (11). The equations can be written as dependent on the current working ratio of the semiconductor  $(d_i = T_c/T_s)$ . These transmission and switching losses equations are given for IGBTs (12) and (13). In these equations, the  $k\omega T_s$  time index, the  $Z_{E-ON}$  and  $Z_{E-OFF}$  transmission, and the energy losses that occur when passing through the cut are the scaled polynomial functions of the residual values at which the key is tested

$$P_{I-C-Ts}[k] = d_i (k\omega T_s) [i_c (k\omega T_s) V_{CE-ON} + i_c^2 (k\omega T_s) R_{CE-ON}(T_j)], \qquad (12)$$

$$P_{I-S-Ts}[k] = f(d_i(k\omega T_s)) \frac{1}{T_s} [Z_{E-ON}(i_c(k\omega T_s)) + Z_{E-OFF}(i_c(k\omega T_s))], \qquad (13)$$

$$f(d_i(k\omega T_s)) \triangleq \operatorname{sgn} \left( f(d_i(k\omega T_s)) \right)$$
$$\times \operatorname{sgn}(1 - f(d_i(k\omega T_s))).$$
(14)

It has been found that the energy conversion efficiency of the system is dependent on the current operation rates of the switches, by associating the fundamental periodic losses of a PES with key parameters and key current/voltage constraints. The current operation ratio remains constant if a PWM-powered power electronics converter only performs DC-DC conversion. In other cases, the current operation rate is variable, and the semiconductor losses of the PES-containing system vary with time with this ratio.

In Fig. 11, the TPSOG method is illustrated by a simple flow diagram. In this diagram, the  $MOSFET_B$  transmission loss is used for the calculation block abbreviation.  $IGBT_B$  transmission loss is used for the abbreviation of the calculation block.  $DIODE_B$  is used for abbreviation of transmission loss calculation block. In these blocks, the switch parameters (AP), the MOSFET  $R_{DS-on}$  value and the switching conditions (EC), the voltage/current constraints, the current operation ratio, and the desired conditions are given as input  $T_e$ . As output, the mean power vector corresponding to each switching period is taken over this period. Once the loss vector of transmission and switching for all the switches has been obtained in this way, the sum of the elements is divided by  $k_{max}$ . The total power lost in the semiconductors is found and the efficiency is calculated depending on the loading index. The same process is obtained in increasing loading indices and a loading-yield graph is obtained up to full load.

# 4. Conclusion

The energy efficiency in power electronic switches (PES) depends on the circuit topology, the semiconductor switching matrix and the passive filter elements and many of their parameters. Estimation of energy efficiency by pre-initial calculation is very important in terms of saving time, effort and resources. In this study, an algorithm for estimating energy efficiency in power electronics converters was proposed and implemented. Through the Switch Selection Algorithm (SSA) method, the transmission and switching losses of the semiconductor power switches are modeled and some calculations are made using the semiconductor circuit element datasheet information. These calculations are first calculated per switching period, then per fundamental period, averaged, then the total losses of the power electronic circuits are found and the efficiency value is calculated. The implementation of the method is that the current work rate functions of the switches need to be known. In the case of various loads of a power electronics converter with the method, the yield is easily calculated. The result of the method is large in terms of sizing, design and performance estimation and it is important in terms of time, labor, material,



Fig. 11. A semiconductor efficiency characterization algorithm for different percentages of power electronic converters.

and welding. The method is particularly useful for the design engineers and the architects.

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