Analytical Threshold Voltage Model Considering Quantum Size Effects for Nanocrystalline Silicon Thin Film Transistors

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This paper presents an analytical model calculating the threshold voltage in nanocrystalline silicon (nc-Si) thin film transistors by considering a granular morphology of silicon nanocrystallites forming the channel and using the two-dimensional the Poisson equation. The numerical calculations demonstrate that, according to the quantum size effects on both dielectric constant and band gap, the threshold voltage values are strongly related to the silicon crystallites structure. To justify the validity of our model suitable for implementation in circuit simulators such as SPICE, the simulation results obtained are compared with the available research data and they shows a satisfactory match, thus, demonstrating the validity of our model.

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1. Introduction

Polycrystalline silicon (poly-Si) thin-film transistors (TFTs) are widely used as switching elements in large scale electronics such as active matrix liquid crystal displays (AMLCDs) [1, 2]. However, due to the high temperature used for crystallization of the amorphous silicon material (about 630 °C) [3, 4] expensive substrates are required for the growth of polysilicon films. Nanocrystalline silicon (nc-Si) has been proposed as a promising alterative material to polysilicon. They have attracted a lot of interests because of their superior properties, such as high doping efficiency, improved carrier mobility, better stability under bias stress or illumination and they can be deposited over a large area at very low temperatures (as low as 120 °C) making nc-Si attractive for fabrication of relatively high quality and inexpensive TFTs compared to those of amorphous and poly-Si [5, 6].

The threshold voltage (V_{th}) of the device is the most important parameter for circuit, device and process characterization. In case of switching transistors of AMLCDs, the threshold performance of the device is required to be studied and monitored continuously. The need for low threshold voltage device arises to save large power dissipation, and to lower the supply voltage while switching to high density packing. By definition, it is defined as the gate voltage at which the device switches from OFF state to ON state and vice versa. In case of device modeling, it is referred to as that particular gate voltage at which the minimum surface channel potential is equal to twice the Fermi potential value [7].

In nc-Si TFTs, there is a difference between threshold voltage and the ON voltage. Basically, the threshold voltage is defined as the gate voltage at which the inversion channel begin to appear within the grain and the ON voltage is defined as the knee of the characteristics [8, 9]. Therefore it is required to develop an accurate model for threshold voltage which will be further useful for the device characterization. Various models [10–12] have been proposed on threshold voltage in poly-Si TFTs however very limited work has been reported in case of nc-Si TFTs. Moreover, it is valuable to study how the threshold voltage in nc-Si TFTs is affected by gate oxide thickness and grain boundary trapping states at different doping density and temperature [13].

Mao [14] has developed a threshold voltage model for nc-Si TFT. A mono-energetic trap state was adopted in the Maos model without any consideration of the geometry of nanocrystallites forming the channel. In the present study, we propose a theoretical approach allowing the threshold voltage analytical calculation by taking into account the channel nanometer crystalline structure in terms of crystallites geometry and size according to the surface potential model already built [15] to determine the electrical field in nc-Si TFTs. A U-shaped density of states is adopted in our model.

2. Theory

Figure 1 shows the schematic view of the device structure assumed for the modeling. It describes the nc-Si TFT three-dimensional channel with a granular morphology characterized by nanometric crystallites size. We consider the silicon nanocrystallites as a set of grains with nanometer sizes and spherical geometry, separated from each others by an amorphous region (grain boundary) [15].

In the inversion layer, the adjacent electrons at channel/gate-oxide interface induced by a positive gate voltage value are trapped into the grain boundary, which causes the depletion region formation within the grains. Then, by applying the Gauss theorem in x and y directions [12], the following equation can be derived:

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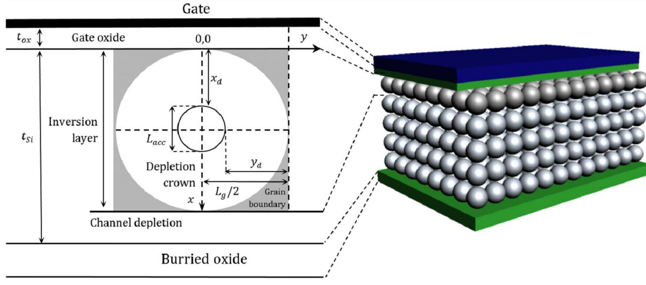

Fig. 1. The cross-sectional view of the channel surface grain in nc-Si TFT [15].

$$\varepsilon_{snc-i}\int_0^{\frac{L_{acc}}{2}}\int_0^{\frac{L_{acc}}{2}}\left(\frac{\partial\psi(x,y)}{\partial x}+\frac{\partial\psi(x,y)}{\partial y}\right)\mathrm{d}x\,\mathrm{d}y$$

$$+C_{ox}\int_0^{y}\int_0^{x}\left[V_{gs}-V_{fb}-\psi(x,0)-\psi(0,y)\right]\mathrm{d}x\,\mathrm{d}y=$$

$$qN_aL_{acc}xy, \tag{1}$$

where L_{acc} is the grain accumulation charge depth, $\psi(x,y)$ is the electrostatic potential, V_{gs} is the gate–source voltage, V_{fb} is the flatband voltage, N_a is the p-type substrate doping concentration, C_{ox} is the gate oxide capacitance per unit area (ε_{ox}/t_{ox}), t_{ox} is the gate oxide thickness, ε_{ox} and ε_{nc-si} are the permittivity of silicon-oxide and nc-Si layer which can be theoretically calculated with the formula below [16]:

$$\varepsilon_{nc-Si}(L_g)=1+\frac{10.4}{1+\left(1.38/10^9L_g\right)^{1.37}}, \tag{2}$$

where L_g is the average grain size in nm.

We assume that the electrostatic potential has a circular distribution with x-axis and y-axis. Therefore [12, 15]:

$$\psi(x,y)=\left[\psi(x,0)+\psi(0,y)\right]$$

$$\times\left[\left(\frac{x}{L_{acc}/2}\right)^2+\left(\frac{y}{L_{acc}/2}\right)^2-1\right], \tag{3}$$

where L_{acc} can be approximated as follows:

$$L_{acc}=\sqrt{\frac{4\varepsilon_{si}\psi_{S0}}{qN_a}} \tag{4}$$

and ψ_{S0} is the potential at the crystallite contact with gate-oxide, given by

$$\psi_{S0}=\frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right)+\frac{E_i-E_v-\chi_0}{q}. \tag{5}$$

E_i is the intrinsic level, E_v is the valence level, n_i is the intrinsic concentration and χ_0 is determined from the following equation [12, 15]:

$$\left[E_g-\chi_0-q\varphi_b\right]N_D^D+N_D^TE_D^T\exp\left[-\frac{\chi_0+q\varphi_b}{E_D^T}\right]=$$

$$N_aL_g \tag{6}$$

where E_g is the band gap, N_D^D is the deep donors states density, E_D^T is the tail donors states level, N_D^T is the tail donors states density and φ_b is the barrier height in the substrate. The trap densities N_A^T and N_D^T are related to the respective grain boundary surface state (areal) density N_{ST} by $N_T=2N_{ST}/L_g$ [10]. The intrinsic carrier density can be obtained as

$$n_i=\frac{2\left(2\pi K\right)^{3/2}}{h^2}\left(m_em_h\right)^{3/4}M_C^{1/2}T^{3/2}$$

$$\times\exp\left(-E_g/2KT\right), \tag{7}$$

where m_e and m_h are the effective masses of electrons and holes respectively, M_C is the number of equivalent minima in the conduction band ($M_C=6$ for silicon), K is the Boltzmann constant, h is the Planck constant and T is the temperature.

Substituting Eq. (3) into Eq. (1), differentiating both sides with respect to x and y, and after some algebraic manipulations, we get the expression of the surface potential in the case of strong inversion as a function of the grain diameter (for $y_d=L_g/2$) which can be expressed as [15]:

$$\psi_S=2\left(V_{gs}-V_{fb}-\frac{qN_aL_{acc}}{C_{ox}}\right) \tag{8}$$

$$+2\left\{\frac{kT}{2q}\ln\left(\frac{N_a}{n_i}\right)-V_{gs}+V_{fb}+\frac{qN_aL_{acc}}{C_{ox}}\right.$$

$$\left.+\frac{1}{2q}\left[\frac{E_g}{2}+\frac{3.4382}{2\times10^9L_g}+\frac{1.1483}{\left(2\times10^9L_g\right)^2-\chi_0}\right]\right\}$$

$$\times\cosh\left(\sqrt{\frac{C_{ox}/\left(2\varepsilon_0L_{acc}\right)}{1+10.4\Big/\left[1+\left(1.38/10^9L_g\right)^{1.37}\right]}}L_g\right).$$

In our approach, the i-th grain in the lateral direction is completely depleted (i.e. $y_d=L_g/2$), the electric field in the channel region is strongly perturbed by the charges at the grain boundary. In this case, we can introduce the following equation in order to report the link between the charge trapped at the grain boundary, the potential distribution at the grain boundary, the electric field and the gate voltage [15]:

$$\varPi\left(V_{gs}-V_{fb}-\psi_{dist}^i-\frac{qN_aL_{acc}}{C_{ox}}\right)$$

$$\times\sinh\left(\varPi y_d\right)=\frac{Q_{GB}}{2\varepsilon_{si}}+E_L, \tag{9}$$

where ψ_{dist}^i is the potential distribution at the i-th grain in the lateral direction, Q_{GB} is the charge trapped at the grain boundary, E_L is the lateral electric field at the grain boundary, and $\varPi=\sqrt{\frac{2C_{ox}}{\varepsilon_{si}L_{acc}}}$ substitution.

The threshold voltage V_{th} of a TFT with finite grain size is defined as the gate voltage at which the minimum surface potential is at the onset of strong inversion or the inversion carrier density at the surface is equal to the background doping concentration N_a. Since the position of the minimum surface potential is near the source, then

ψ^i_{dist} in Eq. (7) is equal to ψ_S. According to Eq. (7) and referring to [12], one can report the threshold voltage expression given by

$$V_{th} = V_{fb} + \frac{\sqrt{2\varepsilon_{si} q N_a \psi_S}}{C_{ox}} + \psi_S + \frac{\psi_S}{\frac{\varepsilon_{si}\Pi}{N_A^D q^2}\sinh\left(\Pi\frac{L_g}{2}\right) + \cosh\left(\Pi\frac{L_g}{2}\right) - 1}, \quad (10)$$

where N_A^D is the deep acceptor state density. This final expression shows the threshold voltage for the nanocrystalline silicon thin film transistor with taking into account the channel granular morphology and the quantum size effects on dielectric constant and bandgap.

3. Results and discussion

The threshold voltage variation as a function of oxide thickness for different trap density values at room temperature described by Eq. (10) is illustrated in Fig. 2 for two different grain sizes (5–20 nm). It is noticed that the threshold voltage increases with the increase in trap density for a given value of gate insulator thickness. This is attributed to the fact that the number of available free carriers for conduction in the channel of the device decrease with increase in trap density. It is also observed that as thickness of gate insulator increases, threshold voltage also increases for all values of trap density. This is due to the fact that as gate oxide thickness increases, the device needs more gate voltage to achieve the strong inversion state in the nc-Si channel layer which forms the channel of the device. From the general trend of the plot, it is seen that the effect of the trap density becomes insignificant at low values of gate oxide thickness. Figure 2 also shows that decrease in grain size from 20 to 5 nm gives rise to short channel effects. This is because decrease in grain size increases the number of grain boundaries or trap centers and the charges trapped in these grain boundaries require extra gate voltage to ionize them thereby increasing the threshold voltage.

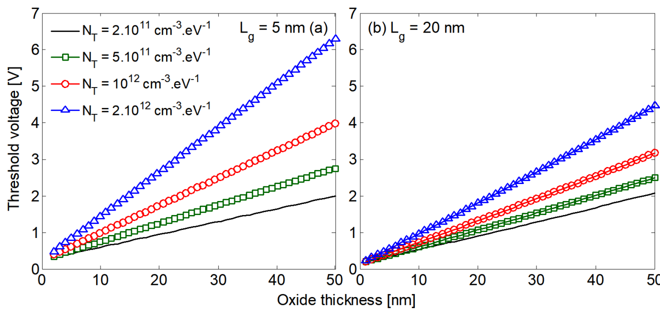

Fig. 2. Variation of threshold voltage as a function of oxide thickness for different values of trap density: (a) $L_g = 5$ nm and (b) $L_g = 20$ nm.

Figure 3 shows the threshold voltage variation with the acceptor doping concentration at different value of gate oxide thickness (at room temperature) for two different grain sizes (5–20 nm). It is observed that the threshold voltage increases with increase of acceptor doping concentration at a given value of gate oxide thickness. Furthermore, it is also observed that the difference in threshold voltage is higher for large values of doping density and it is less in the lower doping concentration. This is attributed to the fact that the trap density becomes important at high doping concentration and these trap states increases the potential barrier across the nc-Si channel and thus degrade the performance of the device.

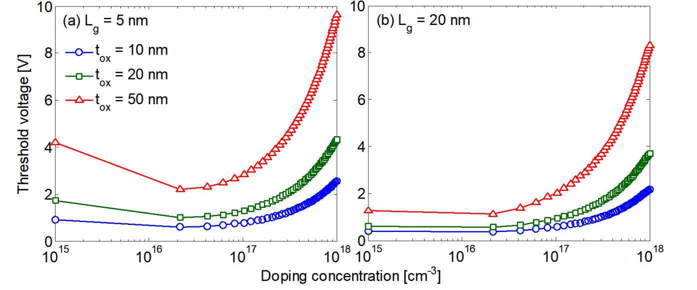

Fig. 3. Variation of threshold voltage as a function of acceptor doping concentration for different values of gate oxide thickness: (a) $L_g = 5$ nm and (b) $L_g = 20$ nm.

The effects of silicon grain size on the threshold voltage and the band gap are calculated and shown in Fig. 4 when the other parameters remain constant at room temperature (300 K). According to Mao's model [14], the physical and technological parameters used for the comparison are taken from [10]. The grain-boundary acceptor trap density, the active doping density, and the flat band voltage have been chosen as 10^{11} cm^{3}eV^{-1}, 10^{14} cm^{-3}, and 1.1 V, respectively. Figure 4 shows that smaller the grain size is, larger the threshold voltage and the band gap will be. With the size of silicon grain decrease, the threshold voltage increases rapidly especially when the size of silicon grain is in the regime of nanoscale (less than 10 nm). Indeed, in this region our model agrees well with experimental data taken from [17]. Moreover, for a TFT with larger grain size (more than 10 nm), the threshold voltage of nc-Si TFTs tends to that of conventional long channel MOSFET.

The surface potential variation as a function of gate voltage described by Eq. (8) is illustrated in Fig. 5. For highlighting the influence of the geometry of silicon crystallites, our simulation results are compared with those obtained by Mao [14].

As shown in the figure and already highlighted in previous work [15], it is clearly seen that initially the surface potential of nc-Si TFTs increases linearly for low gate voltages, then saturates at $V_{gs} \geq 2.4$ V and keeps nearly constant under the strong inversion condition. It is observed that the two curves are in excellent agreement for all values of gate voltage in the weak inversion. The rapid evolution of the surface potential in this region is attributed to the influence of quantum effects through the

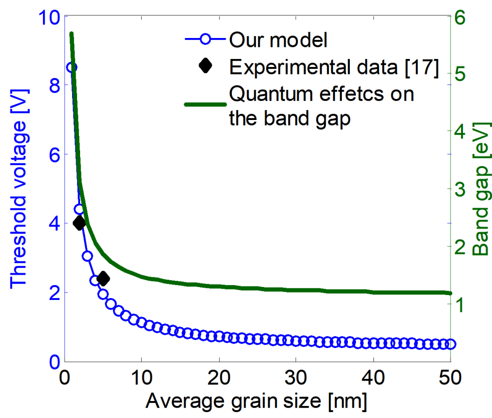

Fig. 4. Threshold voltage and band gap versus the average grain size at room temperature.

dielectric constant, the band gap, and the grain boundaries traps.

However, in strong inversion (for $V_{gs} \geq V_{th}$), a disagreement is observed between the two plots. This is attributed to the fact the quantum size effects becomes negligible and the morphology in terms of grains diameter and geometry, expressed by the hyperbolic cosine function in Eq. (8), becomes dominant in the control of the surface potential variation for higher values of gate voltage.

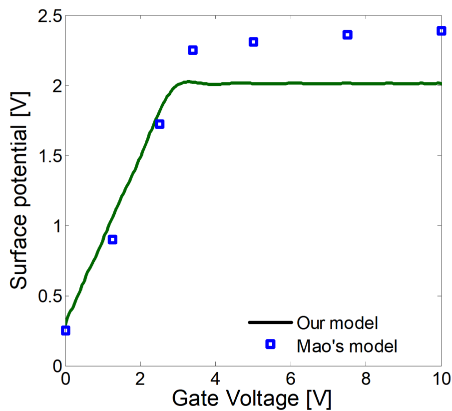

Fig. 5. 5. Surface potential versus gate voltage comparison with the Mao model.

4. Conclusion

In this work, the impacts of the size and the morphology of silicon grain on the threshold voltage have been theoretically investigated. An analytical model has been proposed to calculate the nc-Si TFT threshold voltage by assuming a nanocrystalline channel structure with granular nanocrystallites morphology. Results show that the threshold voltage in nc-Si TFTs strongly depends on the size of silicon grain especially in the regime of nanoscale. The change in both dielectric constant and band gap of nc-Si caused by quantum size effects can largely affect on the channel surface potential and hence on the threshold voltage in nc-Si TFTs. Moreover, the effect of the channel morphology on the threshold voltage has been highlighted for various silicon nanocrystallites sizes.

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