

# Quadrature Oscillator Design with $G_m$ -C Structure

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This paper presents an attractive and new quadrature oscillator based on  $G_m$ -C structure. The proposed quadrature oscillator is achieved with MOS transistors and two capacitors. The passive capacitors are grounded, which is an advantage for integrated circuit implementation. The theoretical results are verified by LTSPICE simulation using the 0.18  $\mu\text{m}$  CMOS technology from TSMC. The proposed quadrature oscillator circuit can be used in several communication and instrumentation systems.

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## 1. Introduction

Quadrature oscillators are important blocks for communication systems, instrumentation systems and signal processing. They provide two sinusoidal outputs with  $90^\circ$  phase difference. In the literature, there are many quadrature oscillators, which were designed with such active elements, as operational transresistance amplifiers [1], current feedback amplifiers [2], current differencing buffered amplifier [3, 4], second generation current conveyor [5], current controlled current differencing buffered amplifier [6], current differencing transconductance amplifier [7], fully differential second generation current conveyor [8], fully balanced voltage differencing buffer amplifier [9]. Furthermore, surface acoustic wave oscillators [10] can be found. Filter design with active element as voltage differencing current conveyor [11] has been also reported.

Circuit realizations of the quadrature oscillators, given in [1], require some floating capacitors, which are not suitable for integrated circuit implementation. In [2–7], the operation requires at least two active elements and three passive components. In [8, 9], quadrature oscillators consist of a single active element and at least three passive components.

In this paper a sinusoidal quadrature oscillator is designed with two active elements and two grounded capacitors, which is an advantage from the integration point of view. The oscillator circuit is designed with  $G_m$ -C topology. A simple operational transconductance amplifier (OTA) and an improved floating current source (FCS) is used to provide  $g_m$  value. The proposed quadrature oscillator is simulated with LTSPICE using the 0.18  $\mu\text{m}$  TSMC CMOS process. Thus, the utility of the proposed circuit is verified.

## 2. The proposed oscillator

The proposed quadrature oscillator is shown in Fig. 1. It is based on  $G_m$ -C topology, where  $g_{m1}$ ,  $g_{m2}$  are

transconductance gains and  $C_1$ ,  $C_2$  are capacitors, which are passive elements.

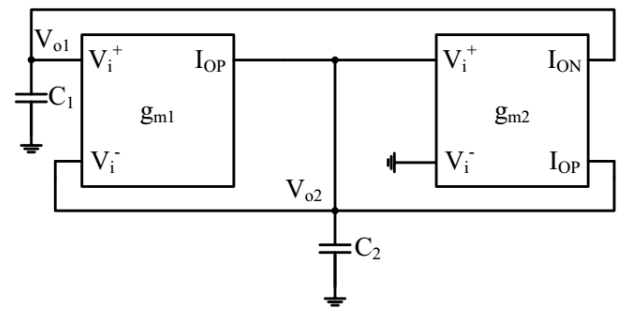


Fig. 1. The proposed quadrature oscillator.

The port relations of the  $g_m$  stage can be described by;

$$I_{OP} = -I_{ON} = g_m(V_i^+ - V_i^-). \quad (1)$$

The characteristic equation of the proposed quadrature oscillator, shown in Fig. 1, can be expressed as follows;

$$s^2 + \frac{(g_{m1} - g_{m2})}{C_2}s + \frac{g_{m1}g_{m2}}{C_1C_2} = 0, \quad (2)$$

It is clearly seen from Eq. (2) that the condition of oscillation and the frequency of oscillations are as follows;

$$\text{CO: } g_{m2} \geq g_{m1}, \quad (3)$$

$$\text{FO: } f_0 = \frac{1}{2\pi} \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}. \quad (4)$$

The relation between the two output voltages of the quadrature oscillator circuit can be calculated as follows;

$$V_{o1} = jk_p V_{o2}, \quad k_p = \sqrt{\frac{g_{m2}C_2}{g_{m1}C_1}}, \quad (5)$$

where  $k_p$  is the voltage ratio among the two output signals of the oscillator. Considering the parasitic impedances of the circuit, the characteristic equation of the proposed quadrature oscillator is recalculated as follows;

$$s^2 + s \left( \frac{1}{C_{T2}R_{P2}} + \frac{1}{C_{T1}R_{P1}} + \frac{1}{C_{T2}}(g_{m1} - g_{m2}) \right)$$

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$$+ \frac{g_{m_1} g_{m_2}}{C_{T_1} C_{T_2}} + \frac{(g_{m_1} - g_{m_2})}{C_{T_1} C_{T_2} R_{P_1}} + \frac{1}{C_{T_1} C_{T_2} R_{P_1} R_{P_2}} = 0, \quad (6)$$

where  $R_{P_1} = R_{PON_2}$ ,  $R_{P_2} = R_{POP_1} || R_{POP_2}$ ,  $C_{T_1} = C_1 + C_{PON_2}$ ,  $C_{T_2} = C_2 + C_{POP_1} + C_{POP_2}$ .  $R_{PO_{ij}}$  and  $C_{PO_{ij}}$  are the parasitic resistances and capacitances, seen at output ports of the circuit, respectively ( $i$  is the negative or positive output port of the  $g_m$  stage and  $j$  is the number of the  $g_m$  stage). From Eq. (6), the effect of the parasitic impedances on the condition of oscillation and on the frequency of oscillations can be defined as follows;

$$\text{CO: } g_{m_2} \geq g_{m_1} + \frac{1}{R_{P_2}} + \frac{C_{T_2}}{C_{T_1} R_{P_1}},$$

$$\text{FO: } f_0 =$$

$$\frac{1}{2\pi} \sqrt{\frac{g_{m_1} g_{m_2}}{C_{T_1} C_{T_2}} + \frac{(g_{m_1} - g_{m_2})}{C_{T_1} C_{T_2} R_{P_1}} + \frac{1}{C_{T_1} C_{T_2} R_{P_1} R_{P_2}}}. \quad (7)$$

The CMOS realization of the proposed oscillator is shown in Fig. 2. Two transconductance stages ( $M_{1-4}$ ,  $M_{5-12}$ ), realized by MOS transistors, provide  $g_m$  values.  $V_{bi}$  provides DC voltage bias and  $I_{bi}$  is the biasing current. For the first  $g_m$  stage a simple OTA circuit is used, because two inputs and one output are required [12]. For the second  $g_m$  stage an improved FCS circuit is used [13]. The output resistance of the improved FCS is higher than that of the FCS, circuit proposed by Arbel and Goldminz [14].

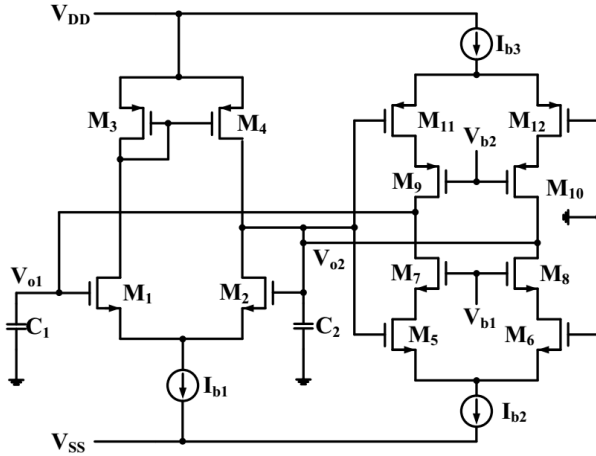


Fig. 2. CMOS realization of the oscillator.

### 3. Simulation results

The proposed quadrature oscillator circuit has been simulated in LTSPICE, using parameters for TSMC of 0.18  $\mu\text{m}$  CMOS process, with  $V_{DD} = 0.9$  V,  $V_{SS} = -0.9$  V. The dimensions of the CMOS transistors are shown in Table I. DC bias voltages are chosen as  $V_{b_1} = 0.3$  V,  $V_{b_2} = -0.3$  V and the biasing currents are chosen as  $I_{b_1} = 100$   $\mu\text{A}$ ,  $I_{b_2} = I_{b_3} = 120$   $\mu\text{A}$ . Transconductance gains  $g_{m_1}$ ,  $g_{m_2}$  are calculated as 488  $\mu\text{A/V}$  and 501.3  $\mu\text{A/V}$ , respectively. It is seen that the value of  $g_{m_2}$  is greater than  $g_{m_1}$ , to ensure the start of oscillations.

TABLE I

Dimensions of the MOS transistors.

Transistors	$W$ [ $\mu\text{m}$ ]	$L$ [ $\mu\text{m}$ ]
$M_1, M_2$	3.6	0.36
$M_3, M_4$	10.8	0.36
$M_5, M_6$	1.8	0.18
$M_7, M_8$	1.8	0.36
$M_9, M_{10}$	8.1	0.36
$M_{11}, M_{12}$	8.1	0.18

The proposed quadrature oscillator, given in Fig. 2, is simulated with the passive capacitors, which are chosen as  $C_1 = C_2 = 10$  pF. The simulation results for output signals  $V_{o_1}$  and  $V_{o_2}$  of the oscillator are shown in Fig. 3a. The quadrature relationship between the generated waveforms has been verified using the plot of  $V_{o_1}$  and  $V_{o_2}$  in X-Y plane in Fig. 3b. The simulated oscillation frequency  $f_0$  for the quadrature oscillator is measured as 7.70 MHz, while the theoretical oscillation frequency is 7.87 MHz. The difference between the two values is due to the parasitic impedances of the circuit. Parasitic resistance and capacitance values of the oscillator are calculated by LTSPICE as  $R_{POP_1} = 72.57$  k $\Omega$ ,  $R_{POP_2} = R_{PON_2} = 1$  M $\Omega$  and  $C_{POP_1} = 16.83$  fF,  $C_{POP_2} = C_{PON_2} = 7.35$  fF, respectively. The total harmonic distortions of  $V_{o_1}$  and  $V_{o_2}$  outputs are 0.58% and 0.71%, respectively.

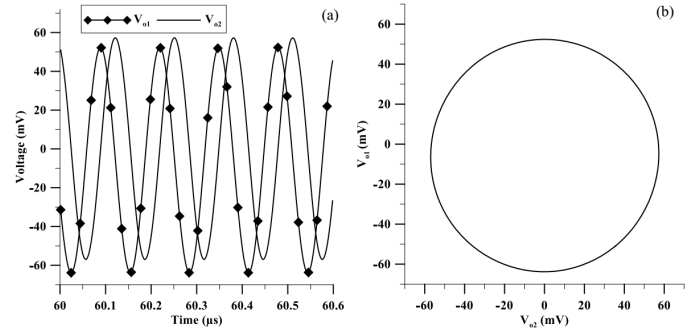


Fig. 3. Voltage outputs of the quadrature oscillator: (a) normal mode (b) X-Y mode.

### 4. Conclusions

In this paper, a quadrature oscillator circuit based on  $G_m$ -C structure is presented. The oscillator is realized with MOS transistors and two grounded capacitors, which is suitable for integrated circuit implementation. The performance of the oscillator is simulated with LTSPICE. Simulation results, obtained using the 0.18  $\mu\text{m}$  CMOS process parameters from TSMC, are provided to verify the utility of the proposed quadrature oscillator. It is demonstrated that simulation results agree well with the theoretical analysis.

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