Special issue of the 3rd International Conference on Computational and Experimental Science and Engineering (ICCESEN 2016)

Electronically Tunable Quadrature Oscillator Employing Single Differential Difference Transconductance Amplifier

A. Yesil[a,*], M. Konal[b] and F. Kacar[b]

[a]Department of Naval Architecture and Marine Engineering, Bandirma Onyedi Eylul University, Balikesir, Turkey

[b]Department of Electrical and Electronics Engineering, Istanbul University, Istanbul, Turkey

In this paper, we present new voltage mode quadrature oscillator, employing single differential difference transconductance amplifier. The proposed oscillator structure consists of two grounded capacitors and a single resistor. The use of grounded capacitors is particularly attractive for integrated circuit implementation. In this way, the frequency of oscillations can be controlled by the biasing current of transconductance stage. Simulation results agree quite well with the theoretical analysis.

DOI: 10.12693/APhysPolA.132.843

PACS/topics: 43.58.Wc, 84.30.Ng

1. Introduction

Quadrature oscillator circuits have a wide range of applications in electronic systems, such as measurement and instrumentation systems, telecommunication systems, instrumentation and single-sideband generators etc. As a result, several realizations of quadrature oscillator circuit, employing active elements, have been reported in the technical literature [1–7].

These quadrature oscillators include realizations using an operational amplifier in [1], current feedback operational amplifier in [2], current differencing buffered amplifier in [3] and [4], differential difference current conveyor in [5], differential voltage current conveyor transconductance amplifier (DVCCTA) in [6] and fully-balanced voltage differencing buffered amplifier (FB-VDBA) [7].

Considering the numbers of active elements in above mentioned voltage mode quadrature oscillators [1–5], it can be clearly observed that at least two active elements and five passive components are required for their realization. In addition, quadrature oscillator circuits in [1, 2] consist of floating capacitor elements, which are not suitable from the integration point of view.

Lahiri et al. [6] presented a voltage mode quadrature oscillator using a single DVCCTA, two grounded resistors and two grounded capacitors. The work by Yesil et al. [7] reported voltage mode quadrature oscillator based on FB-VDBA, employing two grounded capacitors and a floating resistor. However, its condition of oscillation depends on the used resistors. Thus, its frequency of oscillation cannot be easily tuned electronically.

The main intention of this paper is to present DDTA-based voltage mode quadrature oscillator, using a minimum number of passive and active elements. The proposed oscillator consists of a single DDTA, a resistor and two grounded capacitors, which are desirable in IC implementation. In addition, the frequency of oscillations can be adjusted through transconductance gain, without influencing the condition of oscillation. Taking into account the topology of the proposed quadrature oscillator, the CMOS realization of DDTA can be modified in such way, that a simple adder circuit, employing only six NMOS transistors, can be used instead of differential difference stage.

*corresponding author; e-mail: ayesil@bandirma.edu.tr

2. Circuit description

The DDTA was initially introduced by Kumngern [8]. Figure 1 depicts the implementation of DDTA that consists of two essential building blocks, such as the differential difference amplifier (DDA) and dual output-operational transconductance amplifier (OTA).

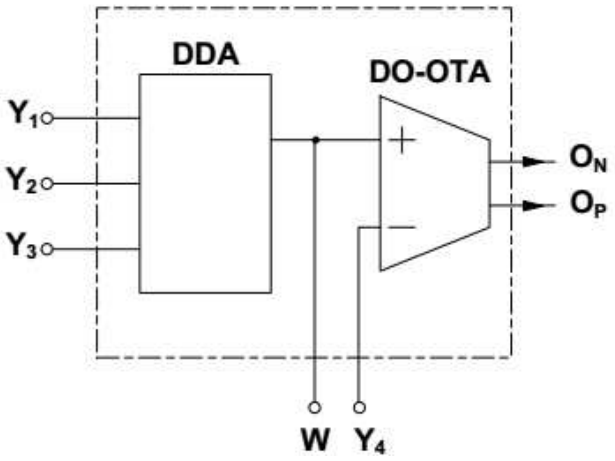

Fig. 1. The implementation of DDTA.

In the mathematical terms, the port relations of the DDTA can be described by $V_W = V_{Y_1} - V_{Y_2} + V_{Y_3}$, $I_{O_P} = -I_{O_N} = g_m(V_W - V_{Y_4})$. The proposed quadrate oscillator circuit is realized by using a single DDTA, two grounded capacitors and a single resistor, as shown in Fig. 2.

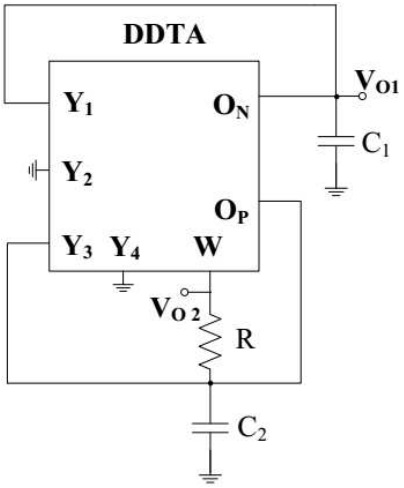

Fig. 2. The proposed oscillator based on DDTA.

The description equations of DDTA and the routine analysis yield the characteristic equation for the proposed quadrate oscillator, shown in Fig. 2, as follows

$$s^2C_1C_2 + sg_m\left(C_2 - C_1\right) + g_mG = 0. \tag{1}$$

It is evident from Eq. (1) that the condition of oscillation and the frequency of oscillations are

$$\text{CO: } C_1 = C_2, \tag{2}$$

$$\text{FO: } f_0 = \frac{1}{2\pi}\sqrt{\frac{g_mG}{C_1C_2}}. \tag{3}$$

It is clearly seen from Eqs. (2) and (3) that frequency of oscillation can be adjusted independently of the condition of oscillation by changing g_m. The relation between the two output voltages of the quadrate oscillator circuit can be calculated as follows

$$V_{O_1} = jk_PV_{O_2}, \;\; k_P = \sqrt{\frac{C_2g_m}{C_1G}}, \tag{4}$$

where k_P is the voltage ratio among two outputs of the proposed quadrate oscillator. Taking into account parasitic impedances of DDTA, the characteristic equation of the proposed quadrate oscillator is recalculated as follows,

$$s^2C_1'C_2' + s\left(g_mC_2' + \left(C_1' + C_2'\right)G_\mathrm{P} - g_mC_1'\right) + g_mG' + G_\mathrm{P}^2 = 0, \tag{5}$$

where $C_1' = C_1 + C_\mathrm{P}$, $C_2' = C_2 + C_\mathrm{P}$ and $G' = 1/(R + R_\mathrm{S})$. The parasitic resistance and capacitance of DDTA, seen at port OP and ON terminal, can be defined by $R_\mathrm{P} = 1/\mathrm{G_P}$ and C_P, respectively. The parasitic resistance, seen at port W, can be described by R_S. Using Eq. (5), the effect of parasitic impedances of DDTA on the condition of oscillation and on the frequency of oscillations can be found as

$$\text{CO: } g_mC_1' = g_mC_2' + \left(C_1' + C_2'\right)G_\mathrm{P}, \tag{6}$$

$$\text{FO: } f_0' = \frac{1}{2\pi}\sqrt{\frac{g_mG' + G_\mathrm{P}^2}{C_1'C_2'}}. \tag{7}$$

3. Simulation results

To verify the theoretical study, the proposed quadrature oscillator was simulated by using LTSPICE. For the simulations, 0.25 μm CMOS technology, provided by TSMC, was used [9]. The CMOS realization of DDA stage of DDTA is realized by pool circuit [8]. The pool circuit consists of two single-ended OTAs. Taking into account the proposed quadrate circuit in Fig. 2, Y_2 terminal is grounded. For this reason, the simpler adder circuit can be used instead of differential difference stage. In this paper, a simple adder circuit, proposed by Minaei et al. [10] was used.

Adder circuit, given in Fig. 3a employs only six NMOS transistors. The CMOS realization of the DO-OTA is also shown in Fig. 3b. The transistor aspect ratios of the adder circuit are $(W/L)_{1-4} = 8\ \mu\mathrm{m}/0.5\ \mu\mathrm{m}$ and $(W/L)_{5-6} = 30\ \mu\mathrm{m}/0.5\ \mu\mathrm{m}$. The transistor aspect ratios of the DO-OTA are $(W/L)_{1-2} = 1.5\ \mu\mathrm{m}/0.25\ \mu\mathrm{m}$, $(W/L)_{3-4} = 1.5\ \mu\mathrm{m}/0.75\ \mu\mathrm{m}$, $(W/L)_{5-8} = 6\ \mu\mathrm{m}/0.75\ \mu\mathrm{m}$ and $(W/L)_{9-12} = 3\ \mu\mathrm{m}/0.75\ \mu\mathrm{m}$. Supply voltages are taken as $V_\mathrm{DD} = -V_\mathrm{SS} = 1.25$ V. Biasing voltage V_B for adder circuit and biasing current I_B for DO-OTA are selected as $V_\mathrm{B} = 0.8$ V and $I_\mathrm{B} = 35\ \mu$A, respectively. Transconductance gain is 623 μA/V, when I_B is set to 35 μA.

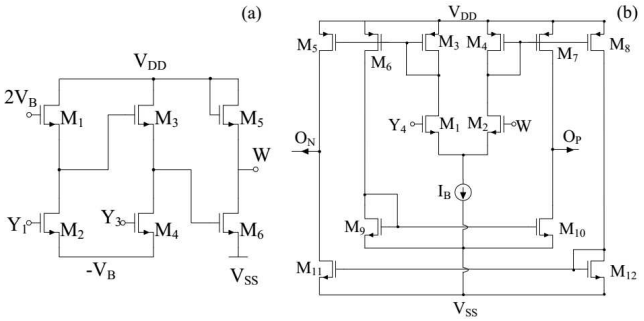

Fig. 3. (a) The CMOS implementation of adder circuit [10]. (b) The CMOS realization of DO-OTA.

Parasitic resistances and capacitance of the adder circuit and DO-OTA were calculated by LTSPICE: $R_\mathrm{S} = 154\ \Omega$, $R_\mathrm{P} = 158\ \mathrm{k}\Omega$ and $C_\mathrm{P} = 0.256$ pF by keeping $I_\mathrm{B} = 35\ \mu$A.

The oscillator has been designed with $C_1 = 105$ pF, $C_2 = 100$ pF and $R = 1\ \mathrm{k}\Omega$. It is seen that the value of C_1 is greater than that of C_2 to ensure the start of oscillations.

Figure 4a and 4b depicts the simulated output waveforms of the quadrature voltage in start-up and steady-state, respectively. The simulated oscillation frequency is 1 MHz, while the theoretical oscillation frequency is 1.22 MHz. The discrepancy between simulated and theoretical results mainly stems from the effects of parasitic impedance of the active elements.

The steady state oscillations were reached within 30 μs. The total harmonic distortions of V_{O_1} and V_{O_2} outputs

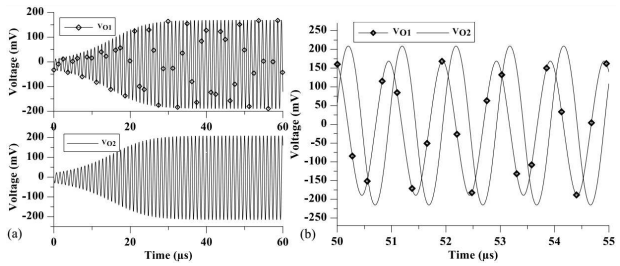

Fig. 4. (a) Start-up and (b) steady state waveform of the quadrature voltage outputs.

are 1.84% and 1.05%, respectively. The oscillation frequency is changed between 0.94 MHz and 1.09 MHz while I_B varies from 20 μA to 80 μA. Lastly, the theoretical and simulated voltage ratio among two outputs k_P can be calculated as 0.77 and 0.84, respectively.

4. Conclusions

In this paper, an electronically controllable voltage mode quadrature oscillator circuit, employing a single DDTA, a single resistor and two grounded capacitors, is presented. The use of grounded capacitors is beneficial to IC implementation. To reduce the number of transistors in the CMOS realization of the quadrature oscillator, the adder circuit is also used instead of differential difference stage. The frequency of oscillations can be tuned by the biasing current of OTA, while the condition of oscillation is ensured by grounded capacitors. It is demonstrated from LTSPICE simulation that the results agree well with the theoretical analysis.

Acknowledgments

This work was supported by Istanbul University Research Fund with the project code 55162. The authors would like to thank Istanbul University Research Fund for this financial support.

References

[1] J.-W. Horng, *Act. Passiv. Electron. Components* **2011**, 320367 (2011).

[2] W. Tangsrirat, W. Surakampontorn, *AEU – Int. J. Electron. Commun.* **63**, 1080 (2009).

[3] A. Lahiri, *J. Circuits, Syst. Comput.* **19**, 1069 (2010).

[4] W. Tangsrirat, D. Prasertsom, T. Piyatat, W. Surakampontorn, *Int. J. Electron.* **95**, 1119 (2008).

[5] M. Kumngern, K. Dejhan, *Act. Passiv. Electron. Components* **2009**, 987304 (2009).

[6] A. Lahiri, W. Jaikla, M. Siripruchyanun, *Analog Integr. Circuits Signal Process.* **65**, 321 (2010).

[7] A. Yesil, F. Kacar, K. Gurkan, *J. Electrical Engin.* **67**, 137 (2016).

[8] M. Kumngern, in: *2012 IEEE Int. Conf. Electronics Design, Systems and Applications (ICEDSA)*, 2012, p. 141.

[9] E. Yuce, S. Minaei, O. Cicekoglu, *Int. J. Electron.* **93**, 533 (2006).

[10] S. Minaei, I.C. Göknar, M. Yıldız, E. Yuce, *Int. J. Electron.* **102**, 911 (2015).