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Electronic Properties of Stacked ZrO_2 Films Fabricated by Atomic Layer Deposition on 4H-SiC

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The electronic properties of ZrO_2/SiO_2 stacked dielectric layers are reported as a function for temperature of the atomic layer deposition process. A dielectric layer has been characterized by $C-V$ and $I-V$ measurements of MIS structures. A strong dependence of κ value of ZrO_2 layer has been observed as a function of deposition temperature T. The values within the range of $\kappa \approx 16-26$ have been obtained. All measured stacked dielectric layers show an increase in dielectric breakdown voltage compared to simple SiO_2 dielectric by average factor of 1.7 and factor of 2 (21 MV/cm) for high–κ oxides deposited at low temperature (85 °C).

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1. Introduction

Silicon carbide (SiC) is a new emerging material for power electronics due to its wide bandgap, high critical electric field and high thermal conductivity [1]. Although SiC can be thermally oxidized resulting in formation of SiO_2 layer, the application of relatively small dielectric constant material ($\kappa_{SiO_2} = 3.9$) leads to a premature breakdown of the MOSFET gate. Since the breakdown mechanism of the device is related to the Gauss law the high–κ dielectrics were proposed as an alternative gate material for SiC power devices [2–4]. Hafnium oxide (HfO_2) [2], aluminum oxide (Al_2O_3) [3] or zirconium oxide (ZrO_2) [4] single dielectric layers have been investigated in recent years for application as gate dielectric. However, two main drawbacks limit a successful implementation: HfO_2 and ZrO_2, materials with dielectric constant higher than that for SiC ($\kappa_{SiC} = 9.66$), have been reported to form relatively small conduction band offset for electrons resulting in an extensive leakage current ($\approx$ 1.07 eV for HfO_2 and $\approx$ 0.94 eV for ZrO_2, respectively [5]). Furthermore, a key parameter for low series resistance of the device — interface state density near the conduction band edge — is still too high for successful application, especially for Al_2O_3 gate dielectric.

This paper presents our investigation of electronic properties for stacked dielectric layers of SiO_2/ZrO_2 fabricated by atomic layer deposition technique (ALD) on 4H-SiC epitaxial layers at different deposition temperature. This approach results in increased critical electric field comparing to thermal SiO_2 and allows for independent optimization of technology for improvement of breakdown voltage and interface properties.

2. Experimental

n-type silicon carbide substrates acquired from Si crystal with lightly nitrogen doped (10^{16} cm^{-3}) epitaxial layer are used as a starting material. These wafers were cleaned using standard RCA procedure with additional dip in buffered HF for native oxide removal. Immediately after the cleaning of the substrates were thermally oxidized at dry O_2 atmosphere at temperature of 1200 °C to form a buffer layer 9±0.3 nm in thickness measured by profilometry. A nickel backside ohmic contact was formed by sputtering and RTP annealing. Then, a high–κ layer was deposited using ALD technique at various deposition temperature within the range of 85–250 °C. The thickness of all high–κ layers was 52±1 nm excluding the process made at 250 °C where the high–κ layer was 64 nm thick. Al-gate MOS capacitors were fabricated using photolithography. A circular capacitors with diameter 200 μm and 50 μm were used for capacitance–voltage ($C-V$) and current–voltage ($I-V$) characterization, respectively. All measurements have been conducted at room temperature.

3. Results and discussion

High frequency $C-V$ curves were measured using Keithley-4200 semiconductor characterization system at 1 MHz to establish the dielectric constant. A normalized characteristics as a function of deposition temperature are shown in Fig. 1.

Dielectric constant was calculated based on accumulation capacitance and measured layer thickness using the Gauss law and neglecting impact of the interface traps. In this case the investigated dielectric stack can be considered as a series connection of two flat-plate capacitors C_{SiO_2} and C_{ZrO_2} where the dielectric constant for ZrO_2 can be calculated from the following equations:

$$\kappa = \frac{C_{ZrO_2} d_{ZrO_2}}{\varepsilon_0 A}, \tag{1}$$

$$C_{ZrO_2} = \frac{C_{SiO_2} C_{ox}}{C_{SiO_2} - C_{ox}}, \tag{2}$$

where d_{ZrO_2}, d_{SiO_2} are high–κ and silicon dioxide layer thicknesses, C_{ox} is accumulation capacitance, A is gate area and ε_0 is electric permittivity of vacuum. All important data used for the calculation are shown in Table I.

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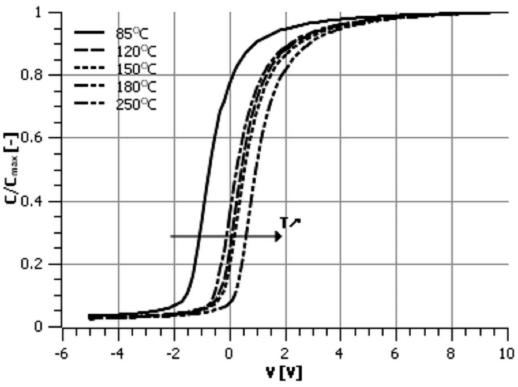

Fig. 1. Normalized $C-V$ characteristics for ZrO_2/SiO_2 dielectric stacks.

The dielectric constant of ZrO_2 layer shows strong dependence on the deposition temperature. The temperatures as low as 85 °C results in a value of $\kappa \approx 16$ reaching the value of $\kappa \approx 26$ known from literature [6] at higher deposition temperature are shown in Fig. 2.

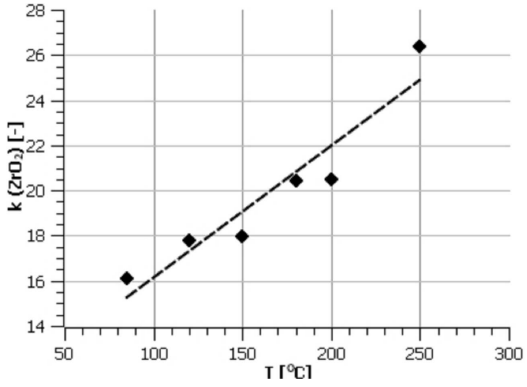

Fig. 2. κ values of ZrO_2 layer as a function of deposition temperature.

TABLE I

Basic parameters of the ZrO_2/SiO_2 dielectric stacks and MOS structures.

τ [°C]	85	120	150	180	250
d_{SiO_2} [nm]	9.1	9.0	8.9	8.7	8.9
d_{ZrO_2} [nm]	51	51	51	53	64
EOT [nm]	21.7	20.0	20.0	18.8	18.6
Φ_B(FN)	2.68	2.64	2.62	2.69	–
U_{fb} [V]	–0.9	0.26	0.29	0.08	0.67
Q_{eff}/q [10^{11} cm^{-2}]	8.78	–2.80	–3.14	–1.06	–7.73

To investigate the usefulness of stacked ZrO_2/SiO_2 layers $I-V$ characteristics were measured using Keithley 4200 semiconductor characterization system. Typical $J(V)$ characteristics are shown in Fig. 3. As can be seen, the conduction mechanism for samples with high-κ dielectrics deposited within temperature range of 85–180 °C are similar with decreasing breakdown voltage for higher deposition temperatures which has been marked

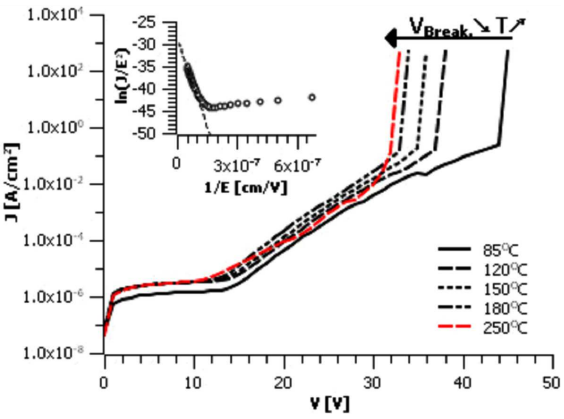

Fig. 3. Typical $J(V)$ characteristics of the ZrO_2/SiO_2 dielectric stacks. Black line — characteristics where the Fowler–Nordheim tunneling is dominant at high field, red line — no Fowler–Nordheim tunneling detected. In the inset — a typical Fowler–Nordheim plot for high–κ layer deposited at 85 °C.

with an arrow in Fig. 3. The sample deposited at temperature of 250 °C shows more complex behavior and it has been highlighted with a red curve. To establish which conduction mechanism is responsible for dielectric stack conduction an electric field in SiO_2 layer was calculated numerically from the Poisson equation. Since the hole concentration is negligible for SiC at room temperature the SiO_2/4H-SiC barrier limits the current density. The main conduction mechanism is dominant one for deposition temperature within the range of 85–180 °C was identified as the Fowler–Nordheim (FN) tunneling described by Eq. (3) for high electric field

$$J_{\mathrm{FN}} = \frac{q^3 E^2}{8\pi h q \phi_B} \exp\left(\frac{-8\pi\sqrt{2qm^*}}{3hE}\phi_B^{\frac{3}{2}}\right), \tag{3}$$

where q is electron charge, h is Planck constant, m^* is electron effective mass for SiO_2 — a value of $m^* = 0.19m$ was used in this study, Φ_B is the barrier height and E is electric field in SiO_2 layer. The presence of the FN tunneling under high field is typical for thermally grown SiO_2 layers known from literature [7]. The barrier height has been extracted from the slope of the $\ln(J/E^2)$ versus $1/E$ plot (shown in Fig. 3 inset for ZrO_2 samples deposited at 85 °C) and shown in Table I. An excellent agreement with theoretical value of $\Phi_B \approx 2.7$ eV has been observed [8] confirming that the SiO_2/4H-SiC interface is limiting current flow at higher electrical field. For sample processed at temperature of 250 °C the FN conduction mechanism has not been identified due to the presence of additional conduction contribution at high electric field indicating probably a different structure of the high–κ dielectric. The critical electrical field in SiO_2 buffer layer was calculated at the breakdown voltage for each sample to compare the dielectric stack breakdown resistance. The critical field as a function of temperature and dielectric constant of the high–κ layer is shown in Fig. 4. All samples show enhanced breakdown properties with an average critical field 1.5–1.7 times higher than

critical field reported in the literature [9] for single layer dielectrics with thickness comparable to the calculated equivalent oxide thickness (EOT) shown in Table I.

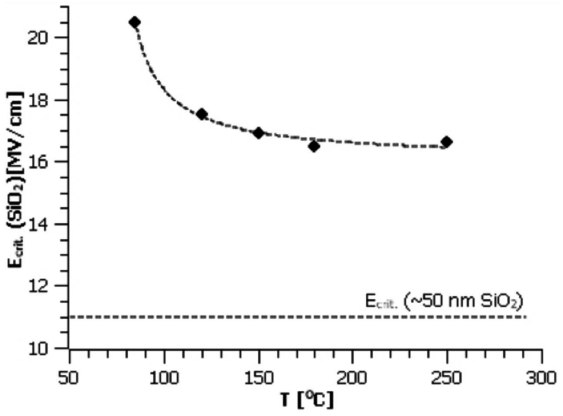

Fig. 4. The calculated critical field in SiO_2 buffer layer under breakdown conditions. The horizontal line indicates a typical critical field for thick single-layer dielectric [9].

The breakdown field also depends on the deposition temperature being as high as 21.3 MV/cm for samples deposited at 85 °C. The breakdown field decreases with increasing deposition temperature reaching the value of $\approx$ 17.3 MV/cm at temperature higher than 150 °C. The obtained results suggest that SiO_2/ZrO_2 stacked layers can be used as a great alternative to simple thermal SiO_2 dielectric structures and resulting in improved breakdown properties of such gate dielectrics. An average increase of the critical field can be addressed to the physics of the breakdown mechanism and the SiO_2 layer thickness [10]. However, the specific increase of the critical field to $\sim$ 17 MV/cm for low deposition temperatures cannot be explained by this hypothesis and has to be related to high–κ layer properties.

The dielectric/semiconductor interface density of states (D_{it}) has been measured for each sample based on high-low method. The trap densities are almost independent of the high–κ deposition temperature and high–κ layer presence typical for SiO_2/SiC interface [11] as expected. Thickness of SiO_2 roughly $\approx$ 9 nm is too high for efficient tunneling of carriers from SiC to ZrO_2/SiO_2 interface. The measured D_{it} profile (not shown here) corresponds to typical for dry thermal SiO_2/SiC [11] having the trap density of 10^{13} cm^{-2} eV^{-1} and decreasing along typical U-shape toward the midgap.

4. Conclusions

High quality ZrO_2/SiO_2 stacked layers have been fabricated by thermal oxidation of 4H-SiC substrates followed by ALD deposition of high–κ dielectrics within temperature range of 85–250 °C. High dielectric constant within the range of $\kappa \approx 16-26$ was obtained for different deposition temperatures. All dielectric stacked layers have excellent breakdown properties that were confirmed by the domination of the Fowler–Nordheim tunneling mechanism at critical electric field. Average critical electric field in the buffer layer of SiO_2 is up to twice larger than for single layer dielectric making this kind of structure more suitable for gate engineering of power MOS devices. An average increase of the critical electric field is provided by thin buffer SiO_2 layer however the dependence of the critical electric field on high–κ deposition process is significant. Another interesting point is poor corelation of critical electric field and trap properties creating the possibility of separate optimization of both parameters. This is a unique beneficial feature of the stack comparing to single layer high–κ dielectrics where ALD deposition process would have to be optimized for both breakdown field and trap properties of dielectric layer simultaneously. This issue need not be taken into account in the case of thermal oxidation followed by ALD deposition.

Acknowledgments

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