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Implementation on Visualization of Some Complex Physics Problems Embodied in Difficulty with Interactive Materials for Undergraduates

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Physical phenomena and the nature of materials require both qualitative and quantitative research to be understood thoroughly. This process often necessitates the use of complicated and expensive equipments. Also in electrical-electronics discipline, especially the nature of semiconductor materials and the behavior of them have a special place. In engineering education, it is often more important for undergraduates to understand the behavior of material and the results of that at the basic level. For this purpose it is sufficient to analyze semiconductor materials with interactive software unlike physics scholars who apply mostly physically to analyze. Understanding the physical properties of applied materials and digitalizing the characteristics of these materials by coding in programming environment maintain its importance. In this context, designing of interactive programs to analyze physical phenomena in electrical-electronics engineering without the need for licensed software has been presented. For this purpose, some semiconductor phenomena involved with electronics engineering have been selected as a pilot and web based 3D Java graphic AWT applications have been designed.

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1. Introduction

The subject matter and many of the concepts in the introductory undergraduate physics courses are abstract and cognitively demanding. Moreover, the underlying mathematical complexity can quickly overwhelm students' intuition [1]. Virtual reality modeling language (VRML) is one of the most effective methods to overcome this problem and give students a comprehensive perception. Both a high level programming language such as Java and VRML can be used to construct materials that provide an almost painless opportunity for beginners to observe simple mathematical models [2]. In this paper, we attempted to clarify some physical problems in terms of semiconductor material modeling commonly encountered in electrical-electronics engineering. Experiments are expensive, time consuming, sometimes hazardous, and usually do not allow much flexibility in parameter variation [3]. The main purpose is to strengthen the conception on material behavior of students without having to use expensive equipments such as electron microscopy. In the following title behavior of p–n junction and the Ebers–Moll modeling of bipolar junction transistor (BJT) were discussed within the scope of virtual reality programming.

2. Some common physics phenomena encountered in electric-electronic engineering

In the assessments made by the scholars in various engineering programs, it is seen that students have deficiencies in the mathematical thinking and problem solving competence. There are also some difficulties at perceptible embodiment of some physics phenomena in electrical-electronics engineering, such as the behavior of the semiconductor materials and magnetic fields. Numerical simulations of p–n junctions usually deal with carrier concentrations and movements while ignoring the mechanical implications of operation of these devices [4]. In this work the theoretical model of a silicon doped p–n diode is developed first and the depletion junction is modeled using diode thermal equations. For this purpose, we have benefited from the results of imaging of the built-in electric field in a p–n junction in a GaAs compound semiconductor by scanning transmission electron microscopy [5].

In the next step, the behavior of BJT is modeled by using the Ebers–Moll parameters. Since a long time SPICE has been the most popular tool dedicated to the simulation, analysis and design of electronic circuits. To do these tasks, the built-in models or library physical models of semiconductor devices utilized in the circuits should be available [6]. The Ebers–Moll parameters are used to model BJT component. The performance of semiconductor devices is strongly dependent on the temperature. SPICE calculations, for any device, run at one, fixed temperature, which typically can be interpreted as the ambient temperature. But the thermal effects are of great importance especially in power devices and therefore in BJTs [6]. Modeling charge carrier distribution in low-doped zones, of bipolar power semiconductor devices, is known as one of the most important issues for accurate description of dynamic behavior of these devices [7]. There are a lot of transistor modeling techniques which use analytical or numerical modules. Also with develo-

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ped nanotechnology, it has gained the great importance of having simulation techniques single-electron transistor (SET/CMOS) hybrid circuits in both dc and transient cases [8]. SPICE uses a general form of the BJT model known as the transport form of the Ebers–Moll model [9]. We have tried to model BJT in a easy way by using the Ebers–Moll parameters and digitalizing of these parameters through computer programming. We will discuss here mathematical behavior of single-element semiconductor silicon, which is in group IV in the periodic table. Each material has almost similar behavior under the same conditions. This shows a strong mathematical relation between the properties of compounds. If we can use this relationship, we can show students how the semiconductor materials behave.

2.1. Behavior of p–n junction

One of the important physical phenomena in electronic circuits is behavior of semiconductor materials. Environment temperature is a major factor affecting the current consumption of an electronic circuit. To simulate and model a silicon based p–n material, at first we must define some mathematical relations. In thermal equilibrium, concentration of free electrons n is equal to the concentration of holes p [9]. If n_i denotes the number of free electrons and holes in a unit volume (cm^3) of intrinsic silicon at a given temperature, it is obtained

$$n = p = n_i = BT^{3/2}\mathrm{e}_g^{-E}/2kT. \tag{1}$$

Here, B is material-dependent parameter, E_g is bandgap energy (the minimum energy required to break a covalent bond) and k is the Boltzmann constant (8.63×10^{-5} eV/K). $B = 7.3 \times 10^{15}$ and $E_g = 1.12$ eV for silicon. As seen in Eq. (1), n_i is a strong function of temperature. If temperature is raised, n_i is also increased.

As known, to increase the concentration of free electrons or holes silicon material is doped with different materials. For n type silicon,

$$p_n n_n = n_i^2.$$

Here, n_n is N_D (donor concentration), where n_i is equal to 1.5×10^{10}/cm^3 at room temperature $T = 300$ K, and for p type silicon,

$$p_p n_p = n_i^2.$$

Here p_p is N_A (acceptor concentration).

For computer simulation, N_A and N_D concentration values can be changed between 10^{15}/cm^3–10^{19}/cm^3. Another semiconductor material component is resistivity of material

$$\rho = \frac{1}{q(p\mu_p + n\mu_n)}, \tag{2}$$

where q is the magnitude of electron charge constant (1.6×10^{-19}), μ_p is hole mobility, μ_n is electron mobility and they are 480 cm^2/(V s), 1350 cm^2/(V s), respectively. As remarked in Eq. (2), it can be seen that resistivity of material reduces while doping factor is increased.

The most important and one of the most effective factors is thermal voltage (V_T):

$$V_T = \frac{kT}{q} = \frac{D_n}{\mu_n} = \frac{D_p}{\mu_p}, \tag{3}$$

where D_p and D_n are diffusion constants for intrinsic silicon, they are 12 cm^2/s and 35 cm^2/s, respectively. The other important parameter for a semiconductor p–n junction component is junction built-in voltage (barrier voltage V_0). V_0 is typically in the range of 0.6 V to 0.9 V for silicon at room temperature.

$$V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right). \tag{4}$$

The another parameter is width of the depletion region. In practical, N_A and N_D concentrations are not equal. So depletion widths are not equal in p–n junction. In Eq. (5) total depletion width W is shown

$$W = x_n + x_p = \sqrt{\frac{2\epsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)V_o}, \tag{5}$$

where $x_n = W\frac{N_A}{N_A+N_D}$ and $x_p = W\frac{N_D}{N_D+N_A}$. $\epsilon_s = 11.7$ is the electrical permittivity of silicon, $\epsilon_0 = 1.04 \times 10^{-12}$ F/cm. In reverse biased p–n junction, depletion region W expands because the reversed voltage V_R is at the same direction of V_0. In that case, in Eq. (5), V_0 is summed with V_R.

For a p–n junction, the another important factor, which affects the I–V characteristic of semiconductor, is reverse saturation current (I_s) caused by diffusion of minority carriers from the neutral regions to the depletion region. I_s is calculated as follows:

$$I_s = Aqn_i^2\left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right)\left(\mathrm{e}^{V/V_T} - 1\right), \tag{6}$$

where A is cross-sectional area of silicon bar, V is reverse or forward biasing voltage, L_p and L_n are diffusion lengths of holes in n material and free electrons in p material, respectively. For simplicity, diffusivity and diffusion length parameters are hold constant and only temperature, A, and dopant variables (N_A, N_D) are changed within certain limits in a 3D graphical AWT based Java application. The change of I_s, W, and V_0 can be tracked as follows. In Fig. 1, the effect of temperature, A, and dopant quantity on width of depletion region, I_s and V_0 are seen. In this case, I_s can be calculated practically by multiplying I_s at room temperature (300 K) with a factor of $(n_i/1.5 \times 10^{10})^2$.

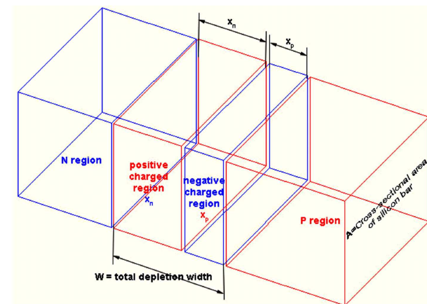

Fig. 1. The effect of temperature, A, and dopant quantity on W, I_s and V_0.

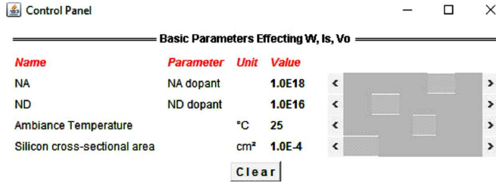

Fig. 2. Control panel for 3D p–n junction simulation.

When 3D Java simulation is worked by control panel in Fig. 2 for the ambiance temperatures at $T_1 = -23\,°\mathrm{C}$ (250 K), $T_2 = 27\,°\mathrm{C}$ (300 K) and $T_3 = 77\,°\mathrm{C}$ (350 K):

$$V_{o1} = 0.875\ \mathrm{V},\ W_1 = 0.39\ \mu\mathrm{m},\ I_{s1} = 7.3 \times 10^{-15} \times (1.5 \times 10^8/1.5 \times 10^{10})^2 = 7.3 \times 10^{-19}\ \mathrm{A},$$

$$V_{o2} = 0.814\ \mathrm{V},\ W_2 = 0.327\ \mu\mathrm{m},\ I_{s2} = 7.3 \times 10^{-15}\ \mathrm{A},$$

$$V_{o3} = 0.748\ \mathrm{V},\ W_3 = 0.310\ \mu\mathrm{m},\ I_{s3} = 7.3 \times 10^{-15} \times (4.1 \times 10^{11}/1.5 \times 10^{10})^2 = 5.5 \times 10^{-12}\ \mathrm{A}.$$

2.2. Ebers–Moll model of bipolar junction transistor

The BJT Ebers–Moll is a transistor model commonly used by some electronic circuit design and analysis programs like Spice and Multisim. There are a lot of constants and parameters affecting the behavior of transistor. While changing these parameters within certain limits, we can get a transistor that behaves like we desire.

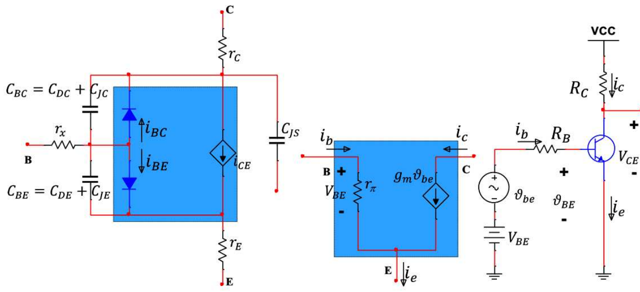

Fig. 3. (a) Small signal model of an n–p–n BJT including the Ebers–Moll parameters, (b) the hybrid-π model for the small signal operation of the BJT, (c) a simple conceptual amplifier circuit of a transistor.

In Fig. 3, small signal model and a conceptual amplifier circuit of an n–p–n BJT are shown. As known, in small signal analysis and at high frequencies internal capacitor effects and the resistance of silicon material of the base, collector and emitter regions should be accounted. The Ebers–Moll parameters for a BJT can be calibrated in the range of these values, as follows: $I_s = 10^{-16}$–10^{-15}, $\beta_F = 50$–200, $\beta_R = 0.1$–2.0, $r_b = 0$–$200\ \Omega$, $r_c = 0$–$100\ \Omega$, $r_e = 0$–$10\ \Omega$, BE junction capacitance = 0.1–1 pF, BC junction capacitance = 0.05–0.5 pF, collector–substrate capacitance is almost zero, BE built-in voltage = 0.6–0.8 V, BC built-in voltage = 0.6–0.8 V, forward transit time $\tau_F = 0$–2×10^{-10} s, reversed transit time $\tau_R = 0$–2×10^{-8} s, $R_C = 100\ \Omega$–$5\ \mathrm{k}\Omega$, $R_B = 10\ \Omega$–$200\ \mathrm{k}\Omega$, ambiance temperature is 50–100 °C.

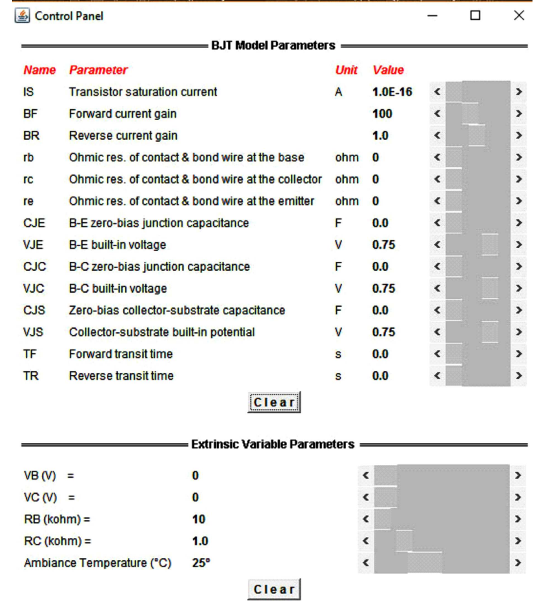

Fig. 4. The Ebers–Moll parameters for BJT.

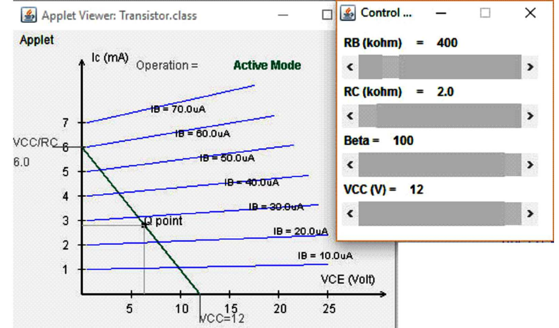

Fig. 5. Drawings of beta curves and calculation of dc Q point of C–E n–p–n amplifier.

In Fig. 4, a Java program code output for the Ebers–Moll parameters of an n–p–n BJT is shown. BE junction and BC junction emission coefficients (n_F and n_R) are not shown and they are assumed to be 1.

By calibrating these values in the given range, we can obtain a desired BJT and analyze this BJT behavior even in high frequencies. Actual transistors, exhibit charge-storage phenomena that limit the speed and frequency of their operation and they can be modeled using capacitances [9].

Specifically, there are two capacitances: the emitter–base capacitance $C_{BE} = C_{DE} + C_{JE}$ and the collector–base capacitance C_{BC}. Here, C_{JE} is zero-bias emitter–base junction capacitance

$$C_{DE} = \tau_F g_m = \tau_F \frac{I_C}{V_T}, \tag{7}$$

$$C_{BC} = \frac{C_{JC}}{\left(1 + \frac{V_{CB}}{V_{CJ}}\right)^m}$$

where

$$m = 0.3\text{–}0.5. \quad (8)$$

For small signal analysis of the circuit shown in Fig. 3c, firstly dc operating values are calculated. In Fig. 5 a sample image view from Java application is displayed.

To draw beta curves, reversed early voltage (V_{AR}) is assumed to be –200 V. After all these applications in Fig. 4 and Fig. 5 are designed, any n–p–n transistor simulation in both high frequency and dc operation can be performed. By adjusting both intrinsic semiconductor material parameters and extrinsic circuit parameters, students in undergraduate education can be easily familiarized with both circuit and component behavior.

3. Conclusions

A number of experiment and applications associated with related discipline were selected to increase the mathematical thinking skills of engineering students who encounter difficulties in physics phenomena, especially related with semiconductor materials. Academic staff tries to arrange education methods in terms of how these kinds of applications would be effective in the increase of students' understandings on the related subjects. They point out that this method could be used in programming classes and it would strengthen the learning activities on related subjects with solution studies. In addition, it has been evaluated that the preparation of applications by graphical based implementation and the simulation of mathematical equations by visualization would contribute to better understanding of physics problems and material behaviors.

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