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An Influence of Silicon Substrate Parameters on a Responsivity of MOSFET-Based Terahertz Detectors

K. Kucharski[a,*], P. Zagrajek[b], D. Tomaszewski[a], A. Panas[a], G. Głuszko[a], J. Marczewski[a] and P. Kopyt[c]

[a]Instytut Technologii Elektronowej, L. Okulickiego 5E, 05-500 Piaseczno, Poland
[b]Military University of Technology, S. Kaliskiego 2, 00-908 Warsaw, Poland
[c]Institute of Radioelectronics, Nowowiejska 15/19, 00-665 Warsaw, Poland

Silicon n-channel MOS transistors are a promising solution for sub-terahertz radiation detection. Their sensitivity is strongly related to the device construction. A type and thickness of the device substrate are key parameters affecting the responsivity, because the silicon substrate is a medium for the radiation propagation and the radiation energy loss, which degrades the detection efficiency. This work is aimed at analysis of the silicon substrate characteristics effect on operation of the MOSFETs as the terahertz radiation sensors. A manufacturing of the MOSFETs on three different substrate types including changing the substrate thickness is described in the paper. Next, the fabricated devices were exposed to THz radiation and their photoresponses were measured. It may be concluded that MOSFETs on silicon-on-insulator wafers with locally thinned substrates demonstrate the highest photoresponse. However, the experiments with the MOSFETs on high resisivity wafers give also promising results.

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1. Introduction

Silicon field effect n-type MOSFETs have been recently used as terahertz (THz) radiation detectors. They are cheap, easy to integrate with silicon read-out and offer reasonable detectivity at room temperature. Their response, i.e. a DC voltage measured between the source and unbiased drain is proportional to a power of an incoming radiation. The response maximum is typically achieved at subthreshold range. The MOSFETs may be easily equipped with patch antennas fabricated on top of the circuit. It has been shown that an effective imaging with use of FETs can be achieved in atmospheric windows of 300 GHz and 600 GHz.

The effective coupling of the FET channel with the THz wave is strongly influenced by the fact that part of radiation is dissipated within the substrate. That may be minimized by thinning the substrate using a grinding technique or by fabricating the detectors on membranes using MEMS-related technologies. Highly resistive substrates may be also used especially if the detector backsides are exposed to radiation via dedicated glued lenses machined using highly resistive silicon. In this paper we examine several types of different substrates to make a suitable choice for a volume production of NMOSFET-based THz detectors.

2. Device manufacturing

The NMOSFETs with polysilicon gate and projected channel length of 3 μm have been used. Their gate and source terminals are coupled with patch antennas designed for 340 GHz frequency. The devices have been manufactured on the following substrate types: on low resistivity Czochralski (Cz-Si) wafers, on silicon-on-insulator (SOI) wafers with low resistivity device layer compatible with CMOS processing and high resistivity handle wafer (to reduce THz power dissipation in the substrate), and on high resistivity floating zone (HR FZ) wafers (Fig. 1). The criteria for material selection are briefly discussed here. It is well known that the response on non-thinned detectors is negligible (even two orders of magnitude smaller) since their substrate acts as a dielectric waveguide. The phenomenon of energy loss mechanisms due to propagation of the electromagnetic wave within the substrate has been described in [1]. For the thick (non-thinned) substrates, several waveguide modes can be propagated within the substrate, even if it is highly resistive, thus less lossy. Then the portion of the power in the air interacting with antenna becomes negligible (see Fig. 3 in [1]). The reason of using the SOI wafers with high resistivity handle wafer is to have an ability to shine the antenna through a highly resistive silicon lens from the backside. Using such an approach we can avoid losses related to the effects described above. However, further discussion is beyond the scope of the paper.

Following the above considerations, the device substrates have been thinned down to 40 μm. In the case of SOI and Cz-Si wafers the membranes have been manufactured using a selective etching, while in the case of HR FZ wafers the grinding technique has been initially used. The selective etching in KOH solution could not have been applied in this case because of the wafer orientation (111). In the complete technological process eight photolithography levels have been used.

*corresponding author; e-mail: kucharsk@ite.waw.pl

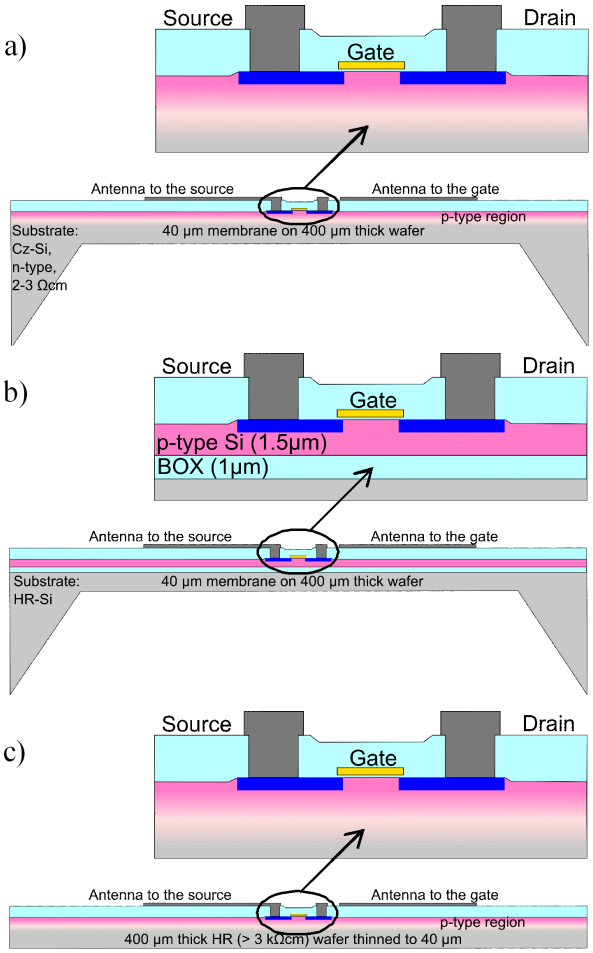

Fig. 1. Cross-sections of n-channel MOSFETs on 40 μm thick substrates: (a) Cz-Si wafer (membrane), (b) SOI wafer with HR substrate (membrane), (c) HR Si wafer thinned via grinding.

3. Measurements

The measurements of the MOSFET responsivity (DC voltage between drain and source) were done. The responsivity was measured with a 340 GHz band transmitter from Virginia Diodes, Inc. as a source of radiation. The frequency multiplier was equipped with a diagonal horn antenna (WR2.8 — full 3 dB beam width of 10°). To measure the detection signal, a lock-in system (Stanford Research Systems SR830) based on modulation at 187 Hz and a low-noise amplifier (SR550) was used. To avoid the interferences, caused by multiple reflections, a very basic measurement setup was used (Fig. 2), without any lenses or mirrors. The radiation frequency was tuned to the resonant frequency of the antenna attached to the source and gate electrodes of the transistor.

The results of the MOSFET photoresponse measurements are shown in Fig. 3. The largest response (100 μV) was obtained for MOSFETs on the SOI wafers with the local membranes. The response of 10÷20 μV was achieved for MOSFETs on the thinned HR silicon wafers. The response of up to 10 μV was achieved for devices on

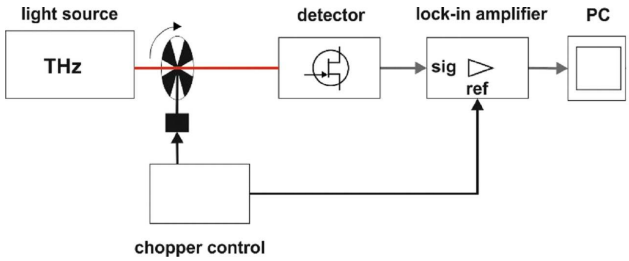

Fig. 2. A block diagram of the setup for measurement of the MOSFET photoresponse to sub-THz radiation.

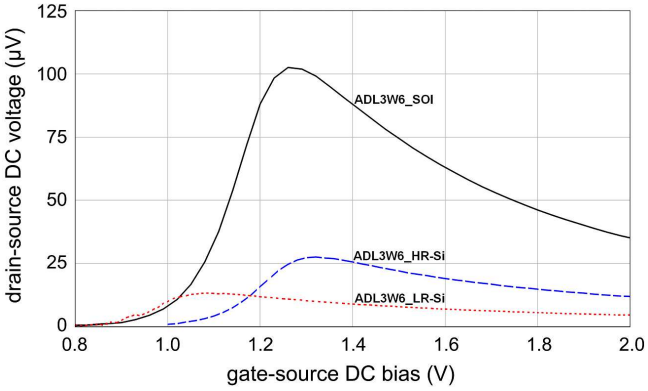

Fig. 3. Typical photoresponse vs. gate voltage characteristics of n-channel MOSFETs on three Si substrates: thick SOI with local 40 μm membranes (solid line), high resistivity Si thinned by grinding (dashed line), and low resistivity Si with local 40 μm membranes (dotted line).

membranes on the Cz-Si wafers. As it was predicted and verified elsewhere, the maximum of the responsivity was achieved in the subthreshold range [2].

It is worth mentioning that in the very recent experiments also the HR FZ (100) wafers have been processed, where membranes have been applied instead of grinding. These devices are under investigation, but the initial measurements of the photoresponse of such sensors are very promising even as compared with SOI devices.

4. Summary

The measurements of the photoresponse of MOSFETs manufactured on different substrate types have been reported. The results demonstrate a high responsivity of the SOI MOSFETs on the membranes. On the HR FZ silicon wafers thinned by grinding the devices reveal lower, though still satisfactory responsivity. The lowest, poor photoresponse has been obtained for the devices on Cz-Si wafers. Recent measurements, which are still in progress, have revealed a high responsivity also for the MOSFETs on HR FZ wafers locally thinned using etched membranes, instead of grinding. This result seems to be interesting because not only the FZ wafer price is significantly lower than of the SOI substrates, but the FZ wafers are easier available as well. So the fabrication of the THz detectors on the HR FZ wafers appears to be

a promising alternative for the SOI-based devices. Currently, further technological experiments are in progress. They are aimed at optimization of the membrane thickness, and at solutions for a more efficient coupling of the MOSFETs with antennas.

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