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Ultra-Low Voltage VDCC Design by Using DTMOS

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In this paper, a new ultralow voltage and ultralow power voltage differencing current conveyor based on dynamic threshold voltage MOS transistors was proposed. The simulations were performed by using LTSpice Program with TSMC CMOS 0.18 μm process parameters. A new notch filter configuration was also presented as an application for the proposed voltage differencing current conveyor. The power consumption of proposed voltage differencing current conveyor was simply 12.42 nW at symmetric $\pm$0.2 V supply voltage. The simulation results were found in close agreement with the theoretical results.

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1. Introduction

The demand for ultralow voltage (ULV), ultralow power (ULP) and high performance electronic devices and VLSI circuits are attracting significant interest for the scientists and special markets and they have grown rapidly. The power consumption has been concerned as a critical parameter particularly for portable electronic devices, medical electronics implant devices, handheld and battery powered devices [1]. Dropping the power dissipation of the circuit is necessary to keep battery life much longer than usual. Reducing the power dissipation is easily and effectively possible by lowering the power supply voltage, however, dropping the supply voltage is causing some problems due to the CMOS evolution. One of them is the signal headroom becoming too small to design circuits with sufficient signal integrity and the other problem is the gate leakage [2]. These problems are hindering the designing ULV and ULP electronic devices. These problems can be fixed by using the dynamic threshold voltage MOS (DTMOS) transistors.

Since most of these physiological signals are very weak in amplitude and relatively low signal-to-noise ratios, the filter design is critical for circuits. The investigations show that the power line interference (50 Hz or 60 Hz) is critical importance during physiological signal recording. Power line noise could be easily picked up through electrode cables, electrical devices and the patient being monitored. Although Twin-T configuration, switched-capacitor integrators [3], operational transconductance amplifiers and capacitors (OTA-C) [4] were extensively employed for low-frequency notch filters, they cannot be easily integrated into silicon.

In this study, the DTMOS transistors based voltage differencing current conveyor (VDCC) circuit and its new notch filter application is proposed. The circuit can be performed by an ultralow supply voltage 0.4 V and it is consuming only 12.42 nW. The transistors have been used in weak inversion for the purpose of the lower power consumption. Because of their good subthreshold slope characteristic, the DTMOS transistors are very desirable for working under the ultralow voltages. According to LTSpice simulations, both VDCC and the proposed filter have performed very well. The proposed DTMOS-based VDCC circuit is suitable for ultralow power, ultralow voltage analogue signal processing, and biomedical applications.

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2. DTMOS based VDCC design

Assaderaghi and others proposed the DTMOS to extend the lower bound of power supply to ultralow voltages [5]. Their proposed DTMOS has a high threshold voltage at zero bias and low threshold voltage at $V_{gs} = V_{dd}$. The body terminal of the transistor is tied to gate terminal to generate the DTMOS transistor. Although PMOS transistors can be connected easily as DTMOS transistor, NMOS transistors require triple-well process which is very expensive process to produce DTMOS transistor with their own wells. Only PMOS transistors are used as a DTMOS in this study, so the restriction limits the overall operation of the proposed circuit where voltage headroom is consumed over the NMOS transistors. The circuit symbol of DTMOS transistor is shown in Fig. 1b.

The symbol of the proposed VDCC circuit is shown in Fig. 1, where p and n are input terminals, and z, x

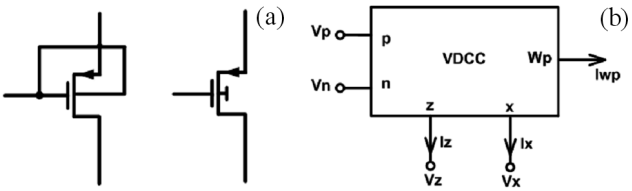

Fig. 1. (a) DTMOS transistor and its circuit symbol [5], (b) block diagrammatic representation of VDCC.

and W_p are output terminals. All of the terminals exhibit high impedance, except the x terminal. The terminal relation of the VDCC can be characterized by the

following matrix:

$$\begin{bmatrix} I_{\rm n} \\ I_{\rm p} \\ I_{\rm z} \\ V_{\rm x} \\ I_{\rm W_p} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{\rm p} \\ V_{\rm n} \\ V_{\rm z} \\ I_{\rm x} \end{bmatrix}. \quad (1)$$

According to the above matrix equation, the first stage can be realized by a balanced transconductance amplifier to convert the difference of the input voltages ($V_{\rm p} - V_{\rm n}$) into the output current ($I_{\rm z}$) with transconductance gain of g_m and the second stage is a current conveyor using for transferring x-terminal current to $W_{\rm p}$ terminal. The internal construction of DTMOS based ULV and ULP proposed VDCC circuit is shown in Fig. 2. This active device consists of an OTA and a current conveyor.

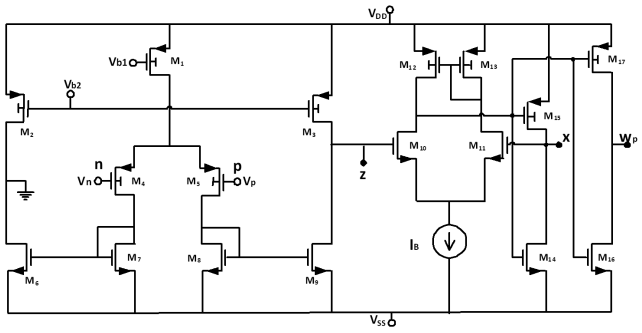

Fig. 2. The proposed DTMOS-based VDCC circuit.

We perform the simulations by using a LTSpice program with TSMC CMOS 0.18 μm process parameters. The aspect ratios of the transistors are given in Table I. Supply voltages are $V_{\rm dd} = -V_{\rm ss} = 0.2$ V and all the biasing voltages are grounded in this application ($V_{\rm b1} = V_{\rm b2} = V_{\rm b3} = 0$ V).

TABLE I

MOSFET dimensions used in VDCC simulations.

Transistor	Width [µm]	Length [µm]
M_1, M_2, M_3,M_{10}, M_{11}	5	2
M_4, M_5, M_{12}, M_{13}, M_{17}	300	2
M_7, M_8, M_{15}	50	5
M_6, M_9	100	5
M_{10}, M_{14}, M_{16}	300	5

The DC transfer characteristics of positive and negative input stages of the proposed active device are shown in Fig. 3. The DC transfer characteristic of $I_{\rm z}$ against $V_{\rm p}$ and $V_{\rm n}$ for VDCC is shown in Fig. 3 that is obtained when the terminal p and n input terminals are grounded, respectively. $V_{\rm x} - V_{\rm z}$ and $I_{W_{\rm p}} - I_{\rm x}$ DC characteristics of the VDCC is shown in Fig. 4. While the lower boundary of the voltage V_x for VDCC is determined as $V_{x\,\rm min} = -199.5$ mV, the upper boundary of voltage $V_{\rm x}$ for VDCC is the positive supply voltage of the VDCC.

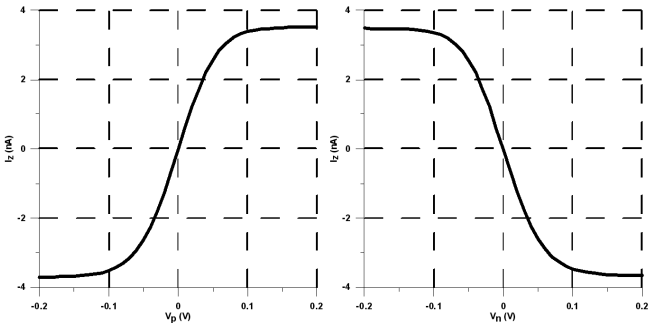

Fig. 3. The DC transfer characteristic of positive and negative input stages of the VDCC.

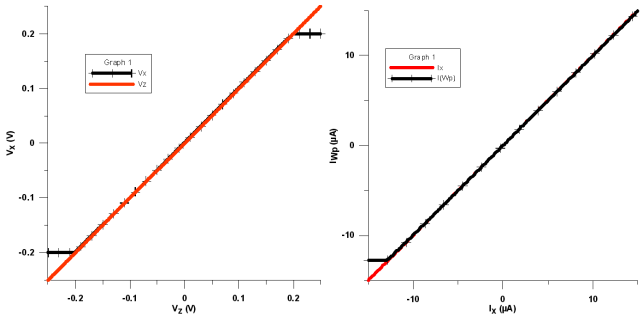

Fig. 4. The DC transfer characteristic of output stage of the VDCC.

While the lower boundary of the current $I_{W_{\rm p}}$ for VDCC is determined as $I_{W_{\rm p}\,\rm min} = -12.5$ μA, the upper boundary of current $I_{W_{\rm p}} = -15$ μA. It can be summarized that input current swing is between –12.5 μA to –15 μA under ±200 mV supply voltages.

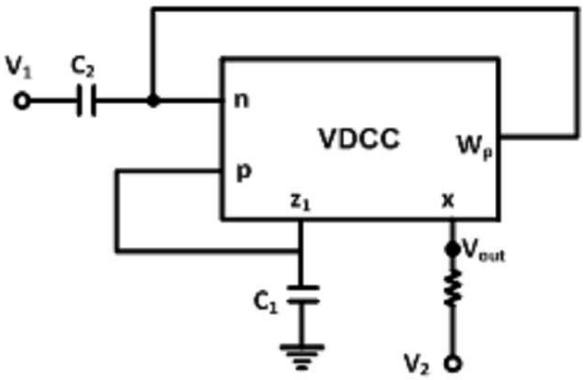

Fig. 5. The proposed filter configuration.

The performance of the proposed active element was tested with an application example of the notch filter which is shown in Fig. 5. The proposed notch filter consists of proposed VDCC device, two capacitors and a resistor. The capacitance values of C_1 and C_2 are 10 pF and 5 pF, respectively. The resistor value is 10 kΩ. The filter's frequency response is shown in Fig. 6. The notch frequency locates at 50 Hz and has an attenuation of 7.7 dB.

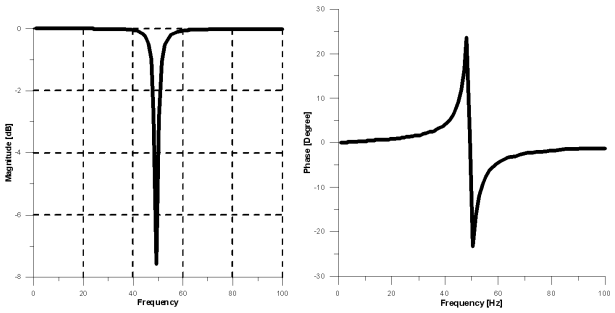

Fig. 6. The simulated results of the proposed filter.

The transfer function (V_{BS}), the pole frequency (ω_0) and the quality factor (Q) are given by Eqs. (2)–(4), respectively.

$$V_{\mathrm{BS}}=\frac{C_1C_2s^2V_1+G_1g_mV_2}{C_1C_2s^2+C_2g_ms+G_1g_m}, \tag{2}$$

$$Q=\sqrt{\frac{C_1G_1}{g_mC_2}}, \tag{3}$$

$$\omega_0=\sqrt{\frac{g_mG}{C_1C_2}}. \tag{4}$$

3. Conclusion

In this study, DTMOS-based VDCC circuit was proposed. The circuit is capable of working a supply voltage 0.4 V and only consuming 12.42 nW, which are suitable value for ultralow voltage and ultralow power operations. For very low power consumption, the transistors were used in weak inversion where DTMOS transistors are very suitable for this mode of operation due to their well subthreshold slope characteristic. The performance of the proposed VDCC was tested with an application example of the notch filter. The simulation results show that proposed notch filter can provide attenuation for the 50 Hz power line interference. The LTSpice simulation results were depicted and according to simulations, both VDCC and filter have performed very well.

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