Proceedings of the 4th International Congress APMAS2014, April 24-27, 2014, Fethiye, Turkey

Compact Modeling of the Performance of SB-CNTFET as a Function of Geometrical and Physical Parameters

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In this work, we study the effects of geometrical and physical parameters on the performances of SB-CNTFET using a compact model. The influences of the physical parameters (height of the Schottky barrier (Φ_{SB}) capacity of oxide layer (C_{INS}) and geometrical parameter (nanotube diameter (d_{CNT})) on the static performance (I_{ON}/I_{OFF}) of SB-CNTFET have been investigated. We present a detailed analysis of the electrical performance of the SB-CNTFET or current-voltage characteristics ($I_D = f(V_{DS})$ for different values of V_{GS}, and also the characteristics ($I_D = f(V_{GS})$) for different values of V_{DS}. All these circuits are studied for a fixed value of $\Phi_{SB} = 0.275$ eV.

DOI: 10.12693/APhysPolA.127.1124

PACS: 85.35.Kt, 85.30.Tv.

1. Introduction

The gradual reduction in the size of silicon transistors (MOSFET) according to Moore's Law is the main stimulus for the integration of more complex circuits. In fact, due to the reduction of the dimensions, the operating speed and integration density of a circuit are increasing. But the miniaturization of MOSFETs makes the manufacturing processes more complex and less reliable. The imperfection of the manufacturing process generates manufacturing defects and it is increasingly difficult to make a circuit with acceptable defect levels. However, the production of flawless circuits is of paramount importance in the field of semiconductors [1].

While the development of CMOS technologies beyond the level of 45 nm continues, certain physical phenomena that were previously insignificant become predominant. These include changes in transistor parameters (dimensions, doping), the variation of the supply voltage and the temperature or leakage currents, the quantum effect and the short channel effect. Parametric variations are the blocking phenomena of the miniaturization. Because of these physical phenomena and limitations of size, silicon-based technology is likely to reach its ultimate limits in 2020, when the channel length of the MOSFET will be less than 10 nm.

A CNT is a sheet of graphite rolled up into a tube. The diameter of a CNT typically varies between 0.4 nm and 3.0 nm and its length may exceed several micrometers [2–4]. The electronic properties of the CNT depend on its geometrical structure. The CNT is a new nano-material interesting for logic applications, and a semiconductor, promising to replace the current silicon. The CNTFET can be mainly based on Schottky barriers present at the metal/CNT junction. The switching occurs by modulation of the contact resistance rather than by altering the resistivity of the channel. The Schottky barrier prevents current through the gate junction at low voltage. When the gate voltage increases, the barrier decreases, so the current can pass through a heat tunnel effect, thus transistor becomes conductive [1, 5–9]. This type of CNTFET is called Schottky barrier CNTFET (SB-CNTFET). It shows a strong ambipolar characteristics.

In this paper, we study the effect of physical and geometrical parameters on the performance of the SB-CNTFET. The relationship between the pass state current I_{ON} and the blocked state current I_{OFF} (I_{ON}/I_{OFF}) is an essential factor for improved static performance of SB-CNTFET. The limitation of the use of this transistor is due generally to the effects of the height of the Schottky barrier (Φ_{SB}), nanotube diameter (d_{CNT}) and the capacity of the oxide layer (C_{INS}). For this reason, we study the effect of the height of Schottky barrier (Φ_{SB}) on the pass state current I_{ON}.

2. Mathematical formulation

A carbon nanotube transistor is formed of two metal contacts, metal/nanotube in drain and source sides. The nature of the metal may be either aluminum (Al), titanium (Ti), palladium (Pd) or scandium (Sc). Platinum (Pt) is often used since it has poor wettability with the carbon nanotubes [10], because it has a low adhesion energy. At the interfaces formed by the metal and the semiconductor nanotube contact, barriers of potential are formed, which prevent the transition of carriers between source and drain through the nanotube channel. Thus, these barriers have an important role in determining the current, since they determine the number of carriers present on the metal side and transmitted in the channel [11].

A change of the polarization of the gate or the drain changes the channel potential, but it also changes the dimensions (height and width) of the two Schottky barriers. Generally, the profile of the band gap close to the contact depends strongly on polarizations V_{GS} and V_{DS}.

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Figure 1 shows a SB-CNTFET structure in "back-gate" configuration for different polarization schemes V_{GS} and V_{DS}. In this example, only the first energy band is shown. Let's examine the variation of the energy band profile and shape of the Schottky barriers depending on the range bias V_{GS} and V_{DS}.

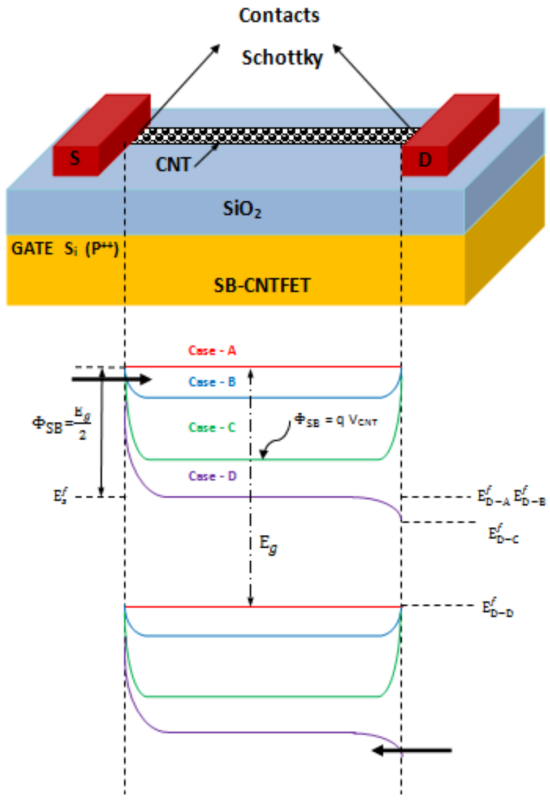

Fig. 1. Schematic representation of energy bands between source and drain of a SB-CNTFET in back gate (top) configuration for different regimes of polarization bands (Case A: $V_{DS} = V_{GS} = 0$, Case B: $V_{GS} > 0 V_{DS} = 0$, Case C: $V_{GS} > V_{DS} > 0$ and Case D: $V_{DS} > V_{GS} > 0$), only the 1st sub-band is shown [12].

2.1. Equivalent electrical circuit

The equivalent electrical circuit for the SB-CNTFET in Fig. 2 follows from the equations of the density of charge of source and drain Q_{QD}, Q_{QS} (Eq. 1) and drain current (Eq. 2)

$$Q_{S,D} = f_{SMO} Q_{\text{low energy}} + (1 - f_{SMO}) Q_{\text{high energy}}, \tag{1}$$

$$I_D = \frac{4ek_BT}{h} \times \sum_{p=1}^{nb-sbbd} \left[\begin{array}{l} \ln\left[1 + \exp \frac{eV_s + \Phi_{SB}^{eff} - sbbd[p]}{k_BT}\right] \\ -\ln\left[1 + \exp \frac{eV_D + \Phi_{SB}^{eff} - sbbd[p]}{k_BT}\right] \end{array} \right]. \tag{2}$$

C_{INS} is the capacity of the gate oxide, it depends on the geometry and the dielectric constant of the insulator;

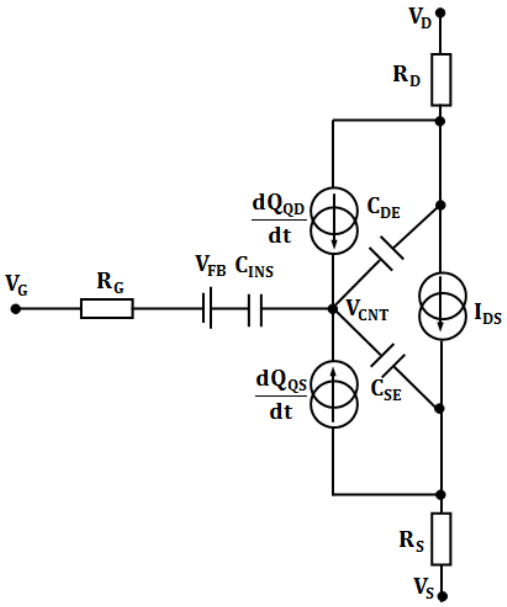

Fig. 2. Schematic of the equivalent model of the carbon nanotube transistor with modulated height barrier [15].

V_{FB} is the voltage of flat bands which takes into account the difference between the work function of the metal and the electron affinity of the nanotube; R_G is the access gate resistance; R_S and R_D are the access resistance of source and drain; C_{SE} and C_{DE} are the electrostatic capacities which represent the change in the load interfaces doped nanotube/intrinsic nanotube. The AC system is obtained from the equivalent circuit [13] and the influence of the barrier Schottky is introduced into the calculation of the current I_{DS} and charge densities Q_{QS} and Q_{QD}.

2.2 Current calculation

The drain current in a SB-CNTFET is calculated using the following equation:

$$I_{DS} = \frac{2e}{2\pi} M \left[\int_0^{\infty} v(k) f_S(k) T_S(E) dk - \int_{-\infty}^{0} v(k) f_D(k) T_D(E) dk \right]. \tag{3}$$

Landauers [14] assume a one-dimensional channel "1D" which is characterized by a ballistic transport between source and drain [15, 16]. Thus I_S is given by

$$I_S = \frac{4e}{h} \sum_{p=1}^{nb-sbbd} \left[\int_{sbbd[p]}^{\infty} \frac{1}{1 + \exp\left(\frac{E - e(V_{CNT} - V_S)}{k_BT}\right)} \times \exp\left(-4 \frac{\sqrt{2m^*}}{3\hbar q E_{doc}} (\Phi_{SB} - E - qV_S)^{\frac{3}{2}} \right) dE \right]. \tag{4}$$

Using the formulation of the effective Schottky barrier, we write:

$$I_{DS} = \frac{2e}{h} M \sum_{p=1}^{nb-sbbd} \times \left[\int_{\Phi_{SB}^{eff}}^{\infty} f_S(E)dE - \int_{\Phi_{SB}^{eff}}^{\infty} f_D(E)dE \right], \quad (5)$$

$$I_{DS} = \frac{4e}{h} \sum_{p=1}^{nb-sbbd} \times \left[\int_{\Phi_{SB}}^{\infty} \frac{1}{1+\exp\left(\frac{E-e(V_{CNT}-V_S)}{k_{BT}}\right)} dE - \int_{\Phi_{SB}}^{\infty} \frac{1}{1+\exp\left(\frac{E-e(V_{CNT}-V_D)}{k_{BT}}\right)} dE \right]. \quad (6)$$

We can integrate the current via the formula [17].

$$\int \frac{dE}{1+b\exp\frac{E}{k_B}} = k_B T \left[\frac{E}{k_B T} - \ln\left(1+b\exp\frac{E}{k_B T}\right) \right] = k_B T \left[-\ln\left(\exp\frac{-E}{k_B T}+b\right) \right] \quad (7)$$

After some simplifications, an analytic result for the drain current in the SB-CNTFET is given by:

$$I_D = \frac{4ek_BT}{h} \times \sum_{p=1}^{-sbbd} \left[\begin{array}{l} \ln\left[1+\exp\frac{eV_s+\Phi_{SB}^{eff}-sbbd[p]}{k_BT}\right] \\ -\ln\left[1+\exp\frac{eV_D+\Phi_{SB}^{eff}-sbbd[p]}{k_BT}\right] \end{array} \right]. \quad (8)$$

With Φ_{SB-S}^{eff} and Φ_{SB-D}^{eff} being the barrier heights of the source and drain, respectively, and defined as

$$\begin{aligned} \Phi_{SB_{S,D}}^{eff} = & \left(\Phi_{SB} - \left(sbbd_{[p]} - eV_{CNT} + V_{S,D}\right)\right) \Phi_{SB_{S,D}}^{eff} = \\ & \left(\Phi_{SB} - \left(sbbd_{[p]} - eV_{CNT} + V_{S,D}\right)\right) \\ & \times \exp\left(-\frac{d_{tunnel}}{\lambda_{schottky}}\right) \\ & + \left(sbbd_{[p]} - eV_{CNT} + V_{S,D}\right) \exp\left(-\frac{d_{tunnel}}{\lambda_{schottky}}\right) \\ & + \left(sbbd_{[p]} - eV_{CNT} + V_{S,D}\right). \end{aligned} \quad (9)$$

3. Results and discussion

In this section we investigate the influence of physical and geometrical parameters on the static performance of the SB-CNTFET.

Figure 3a shows the variation of the drain current I_{DS} with the gate voltage V_{GS}, for various values of height barrier Φ_{SB}. From the Figure, it is observed that for the negative values of gate voltage ($V_{GS} \leq 0$), the current degrades almost linearly and is tending to zero. For positive values of gate voltage and positive ($V_{GS} > 0$), the drain current increases almost linearly. It is also noted that from the characteristics $I_{DS} = f(V_{GS})$, for

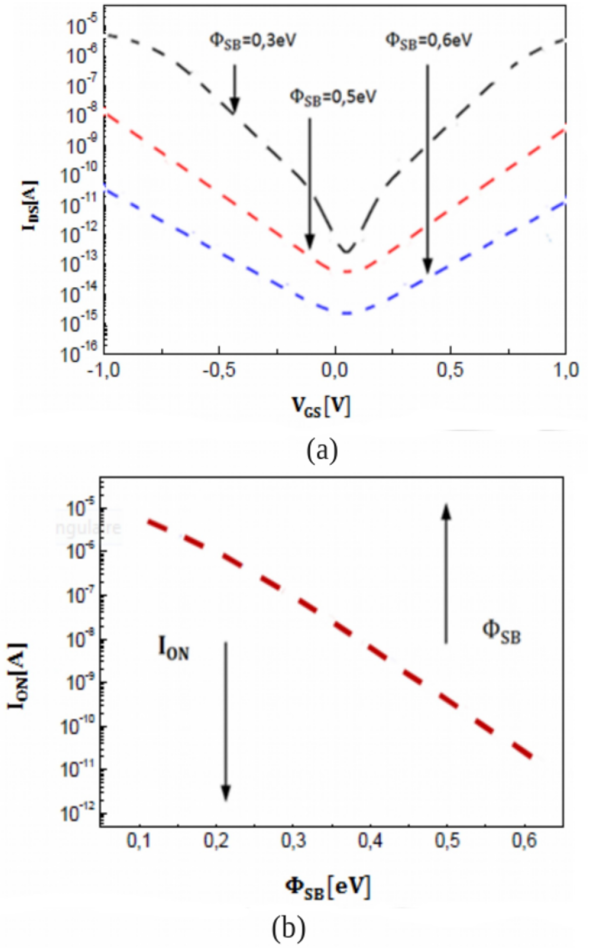

Fig. 3. (a)Variation of drain current I_{DS} versus the gate voltage V_{GS}, for various values of the height barrier Φ_{SB}. (b) the current in the on state I_{ON} versus of the height barrier Φ_{SB}.

the three values of Φ_{SB}, we find that the higher is the barrier, the lower gets current I_{DS}, which gives a low static conduction. Figure 3b shows the characteristics $I_{ON} = f(\Phi_{SB})$. We observe that as the height barrier Φ_{SB} increases the current ot the on-state I_{ON} decreases exponentially, which affects directly the static performance of SB-CNTFET.

Now, we study the effect of geometrical parameter on the structure under consideration. Figure 4a shows the characteristics $I_{DS} = f(V_{GS})$ for two chirality values; (13, 0) and (19, 0). It is observed that the current I_{OFF} increases with the increases of the diameter of SB-CNTFET, this is because the gaps become lower. In Figure 4b, we show the influence of the oxide thickness EOT on I_{on}/I_{off} ratio. We can see that the I_{on}/I_{off} ratio is higher for low oxide thicknesses (C_{INS} capacity). We observe also an important linear variation of I_{on}/I_{off} ratio in the range 1 nm< EOT < 10 nm, this linear variation will be lower in the range 10 nm < EOT < 100 nm. Consequently, we can state that the static performances

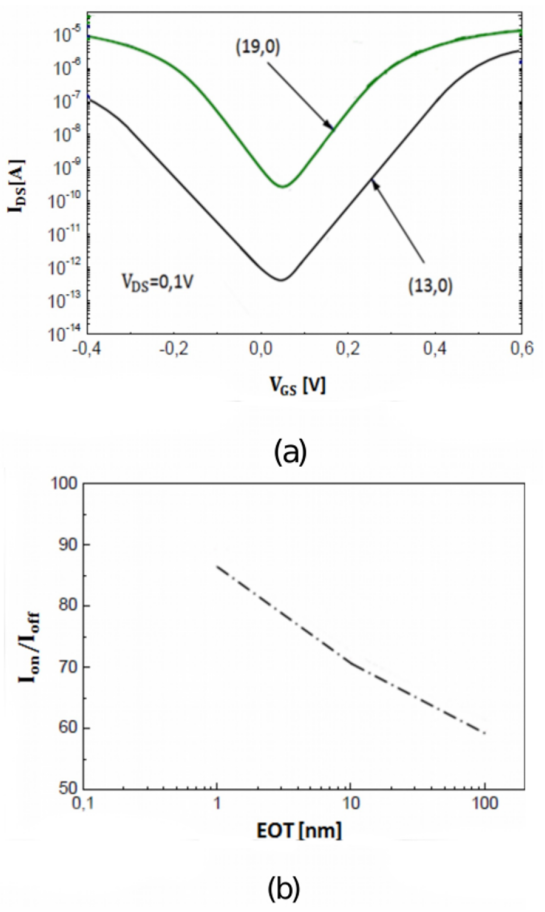

Fig. 4. (a) The characteristics $I_{DS} = f(V_{GS})$ for two chirality values (13, 0) and (19, 0). (b) The characteristics $I_{on}/I_{off} = f(EOT)$.

are enhanced for low EOT thicknesses.

4. Conclusion

The effects of geometrical and physical parameters on the static performances of SB-CNTFET, calculated using a compact model, are reported. Analysis indicates that the static performances of SB-CNTFET are affect by height of the barrier Φ_{SB}. Further results show that the current I_{OFF} is increased with the increase of the diameter of SB-CNTFET. We also demonstrate that the I_{on}/I_{off} ratio is increased with the decrease of the EOT thickness, which enhances the static performances of SB-CNTFET. In future work, the static and dynamic cases will be considered simultaneously for better understanding of performances of the SB-CNTFET.

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