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Improved Transresistance Characteristics of Inductance-gate Type SFFT Using AFM Lithography

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An atomic force microscope (AFM) was used to locally anodize the serial channels of an inductance-gate type superconducting flux flow transistor (SFFT) as narrow slits with a width of 50 μm, a space of 25 μm, and 12 turns, to improve the transresistance value. Among the serial channels that were anodized with the scanning tip of the AFM in the drain current line, channels 1 and 2 were 7.3 and 7.9 μm wide, and 531 and 461 nm high, respectively. The critical current density in the serial channel of the fabricated SFFT, which was determined using an AFM modification method, was decreased by increasing the gate current. The measured current-voltage curves were compared with the simulated ones. The maximum transresistance value was 0.56 Ω at the drain current of 20 mA when the gate current was 6 mA. The transresistance characteristics of the inductance-gate type SFFT could be more improved than that of the single-channel type SFFT using an inductively coupled plasma lithography method

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1. Introduction

Lithography techniques based on scanning probe microscopy (SPM) have been proven to be extremely flexible patterning tools, enabling atomic assembly, chemical patterning, and topological sculpturing [1–4]. Recently, proximal probes such as scanning tunneling microscopy (STM) and atomic force microscopy (AFM) have attracted attention as potential new tools for nano fabrication because of their demonstrated ability to image and manipulate matter at the atomic level [5–6]. Many related studies have been reported since Dagata *et al.* presented the modification of a hydrogen-passivated surface with a scanning tunneling microscope that was operated in air [7].

We tried to fabricate various superconducting flux flow transistors (SFFTs) using AFM [8–10]. Many groups have been studied to improve the transresistance value of the SFFTs [11–13]. Previously, we reported that the transresistance value was 0.3 Ω for a drain current of 51 mA at the gate current of 12 mA, and that the critical current value was 12 mA without the application of the gate current for YBCO single-channel SFFT that was formed using the inductively coupled plasma (ICP) [14]. However, to date, there is no reported research on the improved transresistance characteristics of SFFT that were constructed via localized anodization using an AFM lithography method.

In this paper, we present a fabrication method for an inductance-gate type serial-channel SFFT for the improvement of the transresistance using the selective anodization process that is induced by an AFM. We performed a numerical simulation to determine the theoretical characteristics of an inductance-gate type serial-channel SFFT, which is controlled by a gate current via the modified channel.

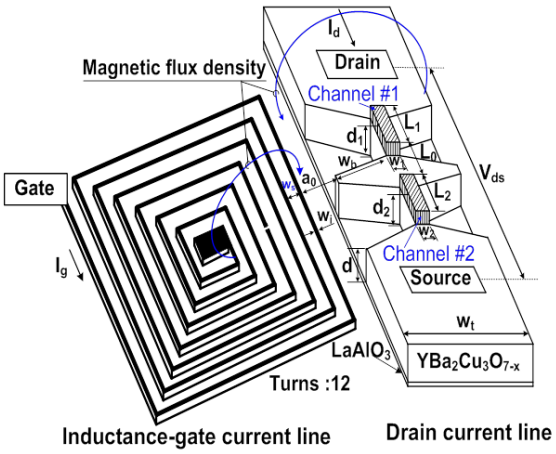

Fig. 1. Scheme of an inductance-gate-type serial-channel SFFT.

2. Experimental

The fabrication scheme for the inductance-gate type serial-channel SFFT is shown in Fig. 1. The inductance-gate type serial-channel SFFT is composed of a serial channel of the drain current line and an inductance gate, as narrow slits of 12 turns at the inductance-gate current line. This SFFT was designed with a 50 μm strip width (w_i), a 25 μm strip space (w_s), a 10 μm space between the strip edge of the inductance-gate current line and the channel edge of the drain current line (a), and a 15 μm parallel length between the external edge and the channel 1 or 2 edge of the drain current line (w_b). The total (w_t) of the drain current line was 40 μm. It contained serial channels 1 and 2 of the drain current line, which were 10 μm wide (w_1 and w_2) and 5 μm long

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(L_1 and L_2), respectively. The vertical length (L) between channels 1 and 2 was 10 μm. We designed this type of SFFT to improve the transresistance value, because the magnetic field that is induced by the current that circulates in a nearby inductance-gate current line supplies the drain current line with the maximum magnetic field without offset each other. When the gate current is applied to an inductance-gate current line, the magnetic flux density in channels 1 and 2 is calculated using Biot-Savart's law at the mean point of the drain current line. To analogize easily the final current-voltage characteristic equation that is induced at the channel terminals of the drain current line, serial channels 1 and 2 should be satisfied with the equilibrium conditions. L_1 and L_2, w_1 and w_2, and d_1 and d_2 of the channel thickness are all equal. The strip width and the strip space at the inductance-gate current line are identical. As a result, the current-voltage characteristic equation that is induced at the channel terminals of the drain current line by the gate current (I_g) of the inductance-gate current line can be written as follows:

$$\begin{cases} V_{ds} = [\frac{4\mu_0(2L_1+L_0)k_BT\delta}{d_1\hbar}\exp^{-(E_P/k_BT)}][I_d - I_{crTi}] \\ \times \sinh[\frac{I_d}{w_1k_BT/(\delta\phi_0)}], \text{ for } I_d \geq I_{crTi}, \\ V_{ds} = 0, for I_d < I_{crTi} \end{cases} \quad (1)$$

wherein k_B and δ are Boltzman's constant and the pinning potential range, respectively, E_p and φ are the pinning energy at temperature (T) and the flux quantum, respectively, μ and $\hbar$ are the permeability of the vacuum and the planck's constant, respectively, I_{crTi} is the total critical current of an inductance- gate type serial-channel SFFT in the drain current line. As the channel length increases, the output voltage increases from Eq. 1. The total critical current varies according to the parameter related to the strip width and space of the inductance-gate current line and the length of the drain current line. When this critical current is the same as or larger than the drain current, the output voltage is induced in the channel by the applied magnetic field, which is generated by the inductance-gate current.

To fabricate the inductance-gate type serial-channel SFFT, a fabrication process is needed, as shown in Fig. 2. The approximately 360 nm-thick superconducting $YBa_2Cu_3O_{7-x}$ (YBCO) thin film was prepared on a $LaAlO_3$ substrate using the thermal evaporation deposition method. The critical temperature (T_c) and the current density (J_c) for the S-type superconducting YBCO thin film were approximately 88.4 K and 2.0 MA/cm^2, respectively. The samples were patterned using a conventional etching method with a photoresist and H3PO4 etchant to fabricate the drain, source, and gate of the SFFT, as shown in Fig. 2. Figure 2a presents the drawing of the mask pattern. Figures 2b and 2c describe the pattern developed using the photo-lithography method, and the photo microscope image of a sample that was fabricated using the wet-etching method with an H_3PO_4 etchant. Figure 2d shows the magnified photo microscope image at the top end of an inductance-gate current line that was formed with the wet-etching method. The space between the drain and the source (see Fig. 2e) in the conventional SFFT was lithographed with an AFM system (Nanoscope IV Multimode, Digital Instruments, Inc., USA) as a channel. Figure 2f presents the topography (see the upper part of Fig. 2f) and phase (see the bottom part of Fig. 2f) images of a serial channel after its oxidization by an AFM bias voltage at –11 V. The applied bias voltage between the sample and an AFM tip was –11 V in the AFM lithograph. The 10×5 μm serial channels were constructed via localized anodization using the AFM lithography method. The AFM was operated

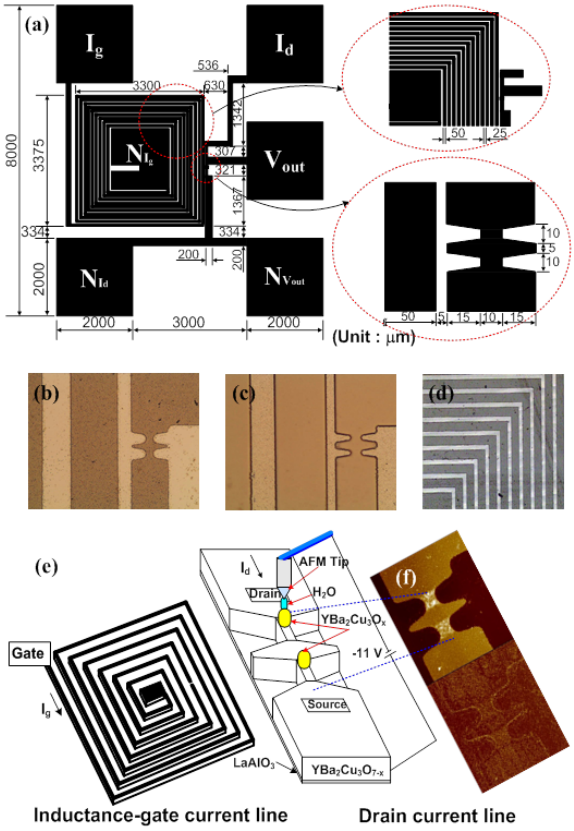

Fig. 2. Fabrication process of an inductance-gate-type serial-channel SFFT by AFM lithography method. (a) Drawing of the mask pattern. (b) Pattern that was developed using the photo lithography method. (c) Photo microscope image of a sample fabricated using the wet-etching method. (d) Magnified photo microscope image at the top end of an inductance-gate current line that was made using the wet-etching method. (e) Fabrication scheme with AFM lithography. (f) Topography and phase image of an inductance- gate-type serial-channel SFFT that was fabricated using the AFM lithography method.

in the contact mode at a force of 10.5 nN, under ambient conditions with a relative humidity of over 50%. The serial channel of the SFFT was modified using a TiOx coating tip, which was biased to a negative voltage with respect to the channel surface, across the 28×7 μm serial channel at a scan rate of 0.83 Hz and a tip velocity of

46.5 μm/s. Highly doped Si cantilevers with 30-nm-thick Ti coating were used as a conducting AFM tips (Mikromasch, Russia).

3. Results and discussion

To investigate the I-V characteristics of an inductance-gate type serial-channel SFFT that was fabricated using the AFM lithography method, we analyzed the modified surface topography with an AFM tapping mode. An AFM image of an inductance-gate type serial-channel SFFT that was fabricated using the wet-chemical etching method is shown in Fig. 3a.

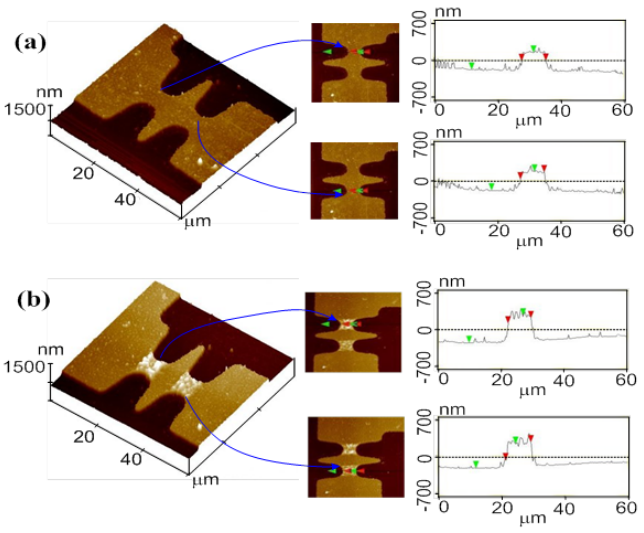

Fig. 3. Section analysis and AFM 3D image of the surface topography (a) before, and (b) after AFM lithography in serial channels 1 and 2.

Figure 4 shows the I-V curves of a serial channel that was modified with the negative bias voltage of –11 V, which exhibited the critical current value of 13 mA without the application of the gate current. When the gate current was increased from 0 up to 6 mA at 1 mA steps in the gate terminals with an inductance structure, the critical current dependence on the gate current decreased significantly, as shown in Fig. 4. The current-voltage characteristic curves are plotted in Fig. 4, and were calculated from the data in the section analysis of the surface after AFM lithography in serial channels 1 and 2.

4. Conclusions

We succeeded in fabricating an inductance-gate type serial-channel SFFT using AFM lithography. The maximum transresistance value was about 0.56 Ω for $I_d = 20$ mA at $I_g = 6$ mA. If this process is applied in the special field of superconducting electronic devices, the AFM modification method can be very useful because it decreases the critical current and does not require an additional wet-etching process. Our results indicated that

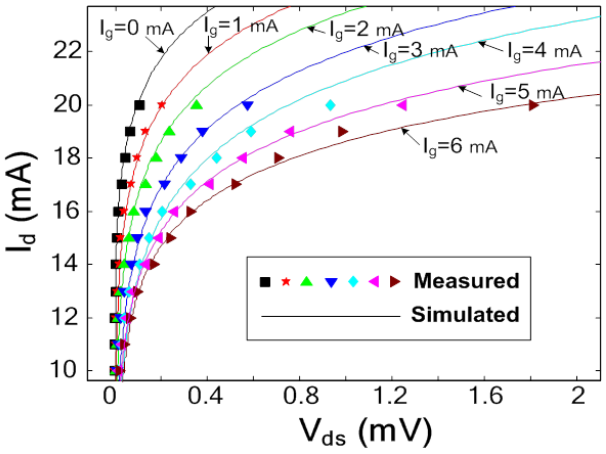

Fig. 4. Current-voltage characteristic curves of an inductance-gate-type serial-channel SFFT that was fabricated using the AFM lithography method.

a serial channel that has an effect as a weak link is effectively fabricated using the AFM lithography method instead of Ar ion milling or ICP. The inductance-gate type serial-channel SFFT is better applied to highly sensitive sensors than digital logic devices because of the large area of the planar rectangular spiral structure.

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