Proceedings of the 43rd "Jaszowiec", International School and Conference on the Physics of Semiconductors, Wisła 2014

The Effect of Phosphorus Incorporation into SiO_2/4H-SiC (0001) Interface on Electrophysical Properties of MOS Structure

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This paper describes the influence of phosphorus incorporation into SiO_2/4H-SiC system. The main scope is an analysis of the slow responding trap states (near interface traps) since the influence of phosphorus technology on fast traps has already been investigated by numerous research groups. Two different phosphorus incorporation methods were incorporated — the diffusion-based process of $POCl_3$ annealing and ion implantation. We have shown that regardless of method used a new distinct near interface trap center can be found located approximately at $E_V + 3.0$ eV. This trap can be related to the incorporated phosphorus amount as shown through secondary ion mass spectroscopy measurements.

DOI: 10.12693/APhysPolA.126.1100

PACS: 81.16.Pr, 77.84.Bw, 77.55.Dj

1. Introduction

The charge trapping properties of silicon dioxide as a gate dielectric in silicon carbide (SiC) MOS structure have been studied extensively for last decade due to its application in electronics Although the experimental results allowed to create the empirical description of the main trap properties as the trap density distribution in the band gap of SiC [1] and many of the detected traps were assigned to the physical defects based on density functional theory (DFT) calculation, the origin of the trap states localized near the conduction band edge of SiC still remains unclear. Nowadays physics of defect creation is described only for simple oxidation technologies in dry oxygen [2–4]. However it was shown that those technologies result in dielectrics that cannot be used in practical applications. Due to that fact it is a common approach to join technological processes with additional elements — nitrogen (N) and phosphorus (P) recently [5–7]. Those techniques were proven to be effective in the reduction of fast trap states [8, 9]. The phosphorus incorporation is considered to be the most suitable for trap density reduction, despite the physical aspects of the process are still poorly understood. Most researchers are focused on reduction of fast trap states measured with conductance and hi-lo CV method. Although the achieved improvement is important due to onresistance decrease of the MOSFETs silicon carbide is known to have high surface concentrations of slow trap states called the near interface traps (NIT). NITs are associated with structural defects localized in the dielectric layer close enough to the interface region and exchanging charge with semiconductor due to tunneling mechanism. Those traps are equally important since they have a strong impact on longterm reliability of MOSFETs. Up to date there is very limited knowledge about the influence of phosphorus incorporation on the NITs. In this work we have investigated phosphorus influence on NITs using two different methods of P introduction.

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2. Experimental

In this work two methods of phosphorus enrichment were used — the high temperature $POCl_3$ annealing and phosphorus implantation to the semiconductor substrate. The 4H-SiC (0001) n-type substrates purchased from SiCrystal were used. The n-type uniformly nitrogen doped epitaxial layer was fabricated with nitrogen concentration of 1×10^{16} cm^{-3} First set of four samples marked #1–#4 was oxidized in dry oxygen at temperature of 1200 °C. Duration of the oxidation process was chosen based on our previous experiments to prevent an excessive growth of oxide thickness and thus maintain the required accuracy of calculated parameters Then, all dielectrics were subjected to high-temperature annealing for 30 min in $POCl_3/O_2$ mixture using nitrogen as a carrier gas at $POCl_3(N_2)$ flow of 273 sccm and O_2 flow of 150 sccm. The second set of samples marked #5–#8 was implanted with phosphorus through thin stopping mask to achieve the shallow implantation profile in SiC substrate. The implantation was performed using ion energy of 100 keV. Samples were not subjected to post-implantation annealing to avoid silicon carbide doping Next the samples were thermally oxidized under the same conditions as the first set. The last sample (#9) was not subjected to any phosphorus process and was only thermally oxidized. This sample is used as a reference. All parameters of the described processes are shown in Table. In case of all samples the dielectric films were used as a gate dielectric in MOS capacitors Those capacitors were

used for electrical characterization using time-dependent CV measurements to extract the response of trap states with long emission time constants (NITs). The electrical response of NITs was investigated based on Fleetwood's method [8], developed and described by Gutt [9]. To correlate the electrical results with the presence of phosphorus, secondary ion mass spectroscopy (SIMS) measurements of investigated samples were carried out.

TABLE I

Technology details for samples used in the experiment. A — implantation dose [$\times 10^{10}$ cm^{-2}], B — implantation energy [keV], C — $POCl_3$ annealing temperature [°C], D — $POCl_3$ annealing time [min], E — oxidation temperature [°C], F — oxide thickness [nm].

	#1	#2	#3	#4	#5	#6	#7	#8	#9
A	–	–	–	–	15	150	1500	15000	–
B	–	–	–	–	100				–
C	950	1000	1050	1100	–	–	–	–	–
D	30				–	–	–	–	–
E	1200								
F	64	83	112	127	42	62	41	27	86

SIMS depth profiles were obtained using Ar+ primary ion beam at 45° incidence angle ion gun system, using Physical Electronics 06-350E. Beam energy was 3 keV and scanning area was set to $1.2 \times 1.7 mm^2$, respectively. The analysis of positive and negative secondary ions was performed using quadrupole mass spectrometer Balzers QMA-410. Since the ionization efficiency coefficients in SiO_2/SiC system with phosphorus are unknown due to unavailability of pure SiO_2/SiC system and matrix effects we have developed the following procedure to estimate the concentration profile shape and levels. Since the calculation of absolute concentration of phosphorus is impossible we have focused on determination of a relative concentration of phosphorus close to SiO_2/SiC interface. A joint current for a given element is expressed by the following equation:

$$I_x = I_0 S^{\gamma} \Omega \tau C_x, \tag{1}$$

where $I_x$is a measured ion current associated with given element, I_0 is primary ion current, S^{γ} is the efficiency of secondary ion emission, Ω is a solid angle of detection, τ is the transmission coefficient of the detection system and C_x is the element concentration.

By calculating the ratio of the two ion currents we obtain expression

$$\frac{I_x}{I_y} = \frac{S_x^{\gamma} \tau_x C_x}{S_y^{\gamma} \tau_y C_y}. \tag{2}$$

Since our research is focused on interface region by selecting the element that can be assumed to have constant relation of $S_P^{\gamma}/S_y^{\gamma}$ and concentration near interface region the ratio of ion current is proportional to concentration of phosphorus [10, 11]. In SiO_2/SiC system this element can be carbon since its concentration is known in bulk material and the oxidation process is carried out with the same conditions in all samples resulting in similar carbon concentration profile near the interface. Therefore all SIMS results are shown here as a ratio of I_P/I_C where the abscissa represents the measurement time. The origin of abscissa is set at the time when the joint beam started to etch SiC bulk calculated as the time when signal rises to 90% of signal gathered from bulk material.

3. Results

The basis for our investigation were electrical measurements performed using capacitance versus voltage stress time method. This method is based on the observation that the trap capturing process can be fully-controlled by the applied voltage and can be much faster than the emission process which is related to the emission coefficient of the specific trap at biasing MOS structure in the depletion region. By applying this negative voltage to our samples for sufficient time all charge trapped by given trap center is emitted resulting in the CV characteristics shift. Measuring both forward and backward CV characteristics the information about this emission process can be extracted by calculating the difference of those two characteristics as originally proposed by Fleetwood and Saks [8]. The detailed physical description of this method can be found in publication of Gutt [9] who developed it specifically for measurements of SiC MOS structures. This method was further modified by our group ensuring the measurement signal parameters fulfilling the same assumptions as in the case of hi-frequency CV methods. In such conditions the voltage point of ΔC maximum associated with a given trap center can be used for the calculation of trap center energy in the bandgap.

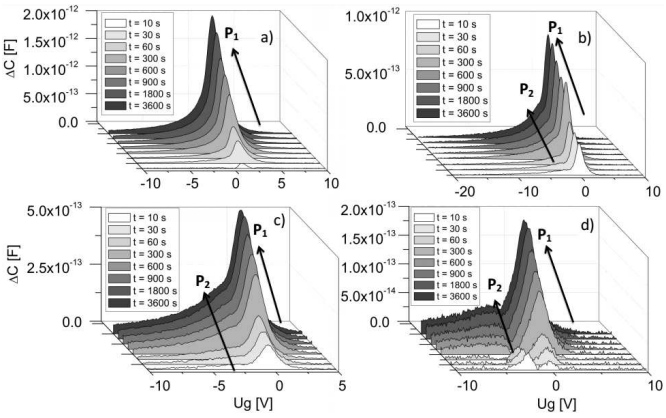

Fig. 1. The ΔC characteristics for samples annealed in $POCl_3$: (a) sample #1, (b) sample #2, (c) sample #3, (d) sample #4.

The result of these measurements for negative voltages biasing times varying from 10 s to 1 h for first set of the samples are shown in Fig. 1. The sample annealed at the lowest temperature shows typical ΔC characteristics with one peak originating from mobile charges in the dielectric layer and border traps with extremely long

emission times. This peak is marked as P_1 With increasing the annealing temperature the additional signal marked as P_2 can be detected Performing deconvolution of the ΔC characteristics using the Lorentz curve fitting the location of this additional peak was calculated at $E_V + (2.9 \div 3.05)$ eV.

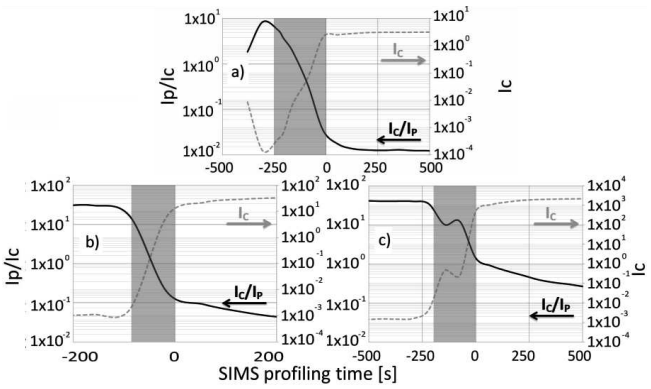

Fig. 2. SIMS measurement profiles for samples annealed in $POCl_3$ ambient: (a) sample #1, (b) sample #2, (c) sample #3.

The presence of the second peak indicates an additional trapping mechanism and the signal is correlated with the amount of phosphorus incorporated at interface region as shown in SIMS measurement profiles in Fig. 2. The darkened region shows profiling time frame when the interface region of SiO_2/SiC structure is being etched As the annealing temperature increases so does the concentration of phosphorus near the interface as indicated by the I_P/I_C signal ratio for samples in the region of interest. It is caused by an enhanced diffusion mechanism at higher temperatures. At the highest temperature phosphorus starts to build up at the interface as shown in Fig. 2c. This sample shows a significant increase of the additional trapping mechanism as shown in Fig. 1. The $POCl_3$ is a complex compound capable of introducing not only phosphorus but also chlorine. Furthermore we have observed an abnormal increase of the oxide thickness during the annealing process which is caused by chlorine penetration of SiC surface. Since rapid oxidation of silicon carbide results in creation of continuous energy profile of NITs the observed signal comprises a plurality of components and the phosphosilicate glass (PSG) related trap (P_2) is only one of them. Therefore it is very difficult to estimate the total amount of charge accumulated at negative bias for 1 h. Moreover, different oxide thickness determines a different negative voltage value to ensure the same surface potential of MOS structure during the negative voltage stress. The value can be even higher than the breakdown voltage. In this work, a constant voltage approach was used To exclude these effects similar measurements were performed at the second set of samples. Since those samples were implanted with phosphorus and no additional impurities were introduced into the structure no rapid oxidation process was present thus the aforementioned effects would not occur.

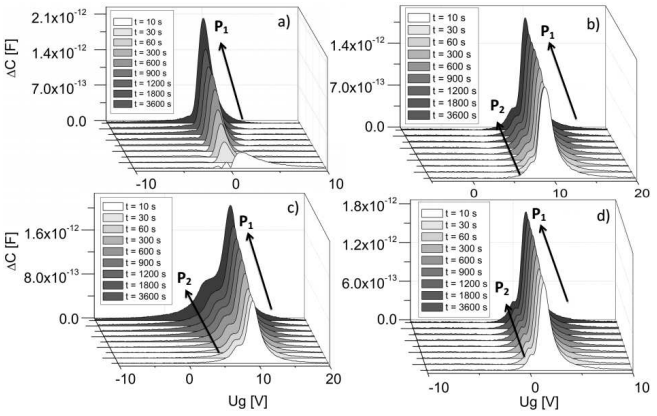

Fig. 3. The ΔC characteristics for samples annealed in $POCl_3$: (a) sample #5, (b) sample #6, (c) sample #7, (d) sample #8.

The results of time-dependent capacitance–voltage measurements of the second set, similar to those shown in Fig. 1, are presented in Fig. 3. As it has been previously demonstrated the results for sample #5, implanted at the smallest dose show only one peak of ΔC characteristics. This is due to small phosphorus concentration in this sample as can be seen on SIMS measurement results in Fig. 4. Samples #6–#8 have approximately one order

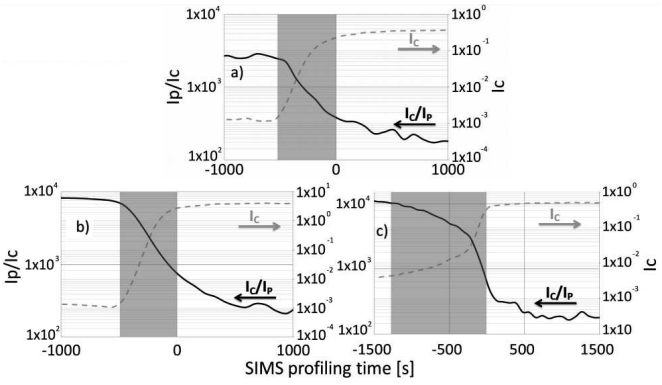

Fig. 4. SIMS measurement profiles for samples implanted with P: (a) sample #5, (b) sample #6. (c) sample #7, (d) sample #8.

of magnitude higher phosphorus concentration comparing to sample #5. Those samples show the presence of the P_2 peak (Fig. 3). The energy location of P_2 peak was calculated at $E_V + (2.93 \div 3.04)$ eV and it corresponds to the first set of samples. However, unlike in the previous set there were no P accumulation at interface effect which was observed for sample #4. In complete contrast to $POCl_3$-based processes described above, P implantation does not cause a quasi-continuous trap profiling, only additional maxima introduced by phosphorus incorporation. In this case, it was possible to estimate the charge accumulated for 1 h accurately based on [8] due to

sharp, additional peak from the introduced phosphorus incorporation. The calculated charge as a function of P concentration is estimated based on SIMS measurement and shown in Fig. 5. The accumulated charge for 1 h stress time is closely correlated to P concentration.

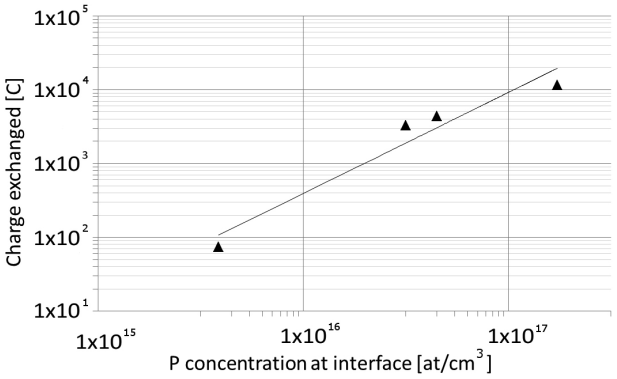

Fig. 5. The estimation of charge exchanged during 1 h voltage stress time versus P concentration at the interface of MOS structure.

4. Discussion

Up to date there are limited reports concerning trap passivation mechanism involving phosphorus. Most investigations considered fast responding traps analyzed by conventional *CV* methods or MOSFET mobility measurements [12–14]. The NITs origin correlated with the presence of phosphorus has not been reported yet. In most cases these traps originate from interface traps ingrowth into the reconstructed oxide forasmuch as the progressive oxidation process constantly consumes the substrate material. Moreover, the defect responsible for NITs formation has to be stable in SiO_2 matrix and this general condition significantly reduces the number of possible candidates. The passivation of the interface states by phosphorus has been related to carbon defects passivation by replacing C atom in threefold coordinated carbon defect by P or P=O [14] or passivation of carbon and silicon dangling bonds at the interface [3, 4]. Since the threefold coordinated carbon defect has been shown to be stable in silica matrix [4] and being able of "growing" into oxide. This defect was suggested as the main cause for NIT traps formation in simple dry oxidation process. Up to date only the dangling silicon bond defect was confirmed by theoretical calculations [15]. This is interface defect but it can result in forming PSG compound near the interface region. In fact, XPS measurements of SiO_2/SiC interface with phosphorus have shown a presence of phosphorus $2p$ peak at 133.9 eV which is in conformity with the spectrum of the P^{5+} state [16]. Our results does not confirm the correlation between SIMS signal from carbon and phosphorus thus the forming of P=O or other PSG compounds is the most probable cause. Since our findings show that the creation of the described defect needs structural rearrangement we conclude that the most probable origin of this defect is phosphorus bonded to dangling Si bonds forming PSG glass during rearrangement However the nature of this defect needs further investigation.

Acknowledgments

This paper was partially supported by the National Science Centre (Poland) grant No. UMO-2012/05/N/ST7/02035. This work was co-financed by European Social Fund.

References

[1] V. Afanasev, M. Bassler, G. Pensl, M. Schulz, *Phys. Status Solidi A* **162**, 321 (1997).

[2] J.M. Knaup, P. Deak, T. Frauenheim, *Phys. Rev. B* **72**, 115323 (2005).

[3] J.M. Knaup, P. Deak, T. Frauenheim, *Phys. Rev. B* **71**, 235321 (2005).

[4] X. Shen, S.T. Pantelides, *Appl. Phys. Lett.* **98**, 053507 (2011).

[5] P. Jamet, S. Dimitrijev, P. Tanner, *J. Appl. Phys.* **90**, 5058 (2001).

[6] G. Gudjonsson, H. Ólafsson, E. Sveinbjörnsson, *Mater. Sci. Forum* **457-460**, 1425 (2004).

[7] D. Okamoto, H. Yano, K. Hirata, T. Hatayama, T. Fuyuki, *IEEE Electron. Dev. Lett.* **31**, 710 (2010).

[8] D.M. Fleetwood, N.S. Saks, *J. Appl. Phys.* **79**, 1583 (1996).

[9] T. Gutt, in: *Proc. 33rd Int. Convention MIPRO 2010*, Eds. P. Biljanovic et al., Croatian Society for Information and Communication Technology, Opatija 2010, Vol. 1, p. 48.

[10] P. Konarski, A. Mierzejewska, *Appl. Surf. Sci.* **203**, 354 (2003).

[11] P.C. Zalm, *Vacuum* **45**, 753 (1994).

[12] D. Okamoto, H. Yano, T. Hatayama T. Fuyuki, *Appl. Phys. Lett.* **96**, 203508 (2010).

[13] R.P. Devaty, M. Dudley, T.P. Chow, P.G. Neudeck, *Mater. Sci. Forum* **717-720**, 739 (2012).

[14] Y.K. Sharma, A.C. Ahyi, T. Issacs-Smith, X. Shen, S.T. Pantelides, X. Zhu, L.C. Feldman, J. Rozen, J.R. Williams, *Solid State Electron.* **68**, 103 (2011).

[15] S. Salemi, N. Goldsman, A. Akturk, A. Lelis, in: *Proc. Int. Conf. on Simulation of Semiconductor Process and Devices SISPAD 2012, Denver*, IEEE, Piscataway 2012, p. 121.

[16] D. Okamoto, H. Yano, S. Kotake, T. Hatayama, T. Fuyuki, *Mater. Sci. Forum* **679**, 338 (2011).