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# A Structural Characterization of GaAs MBE Grown on Si Pillars

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Growth on deeply patterned substrates, i.e. on pillars instead of a continuous substrate, is expected to be very promising to get crack free epilayers on wafers without any bowing. We report here on a structural investigation of GaAs MBE deposited on patterned (001) offcut Si, consisting of pillars 8  $\mu\text{m}$  high and 5 to 9  $\mu\text{m}$  wide, to check mostly the behaviour of the threading dislocations. It is found that only very rarely they propagate up to the GaAs top that will serve as active region in devices. Twins were also detected which sometimes reached the topmost part of GaAs. However, as twins have no associated dangling bonds, they should not be electrically active. Rare antiphase boundaries exist at the interface, hence not harmful for device operation.

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## 1. Introduction

The heteroepitaxial growth of III–V semiconductor layers on lattice mismatched substrates is known to result in misfit (MD) and threading dislocations (TD) forming during relaxation of the misfit strain [1–5]. Additional problems arise for device applications in which the epitaxial structures have to be thick, such as in multi-junction solar cells, high brightness light-emitting diodes (LEDs) and power transistors. Here, different thermal expansion coefficients of layers and substrates often cause wafer bowing [6] and layer cracking [7, 8]. These may prohibit further wafer processing and/or cause device failure. The mismatch problem is especially relevant for the monolithic integration of optoelectronic devices from III–V semiconductors with CMOS-processed Si substrates which has become an area of immense interest in the past two decades and more [9–11]. Much work has been done to reduce the density of the MDs and TDs both theoretically [1, 2, 12–15] and experimentally [5, 16, 17]. One of the most promising approaches to date appears to be the method of aspect ratio trapping [4] followed by lateral overgrowth [18]. Upon coalescence new TDs are inevitably formed and eventually cracks appear as the layer thickness increases owing to the thermal stress.

It has been shown recently that space filling arrays of

Ge microcrystals up to 50  $\mu\text{m}$  in height can be grown on Si substrates deeply patterned at the  $\mu\text{m}$  scale [19], i.e. on Si pillars. By growing on pillars instead of a continuous substrate the thermal strain is completely relaxed thanks to the finite gaps between the Ge crystals, such that neither cracks nor significant wafer bowing can occur [19]. Here we apply this approach to the growth of GaAs microcrystals on Si pillars, for which the lattice mismatch and the mismatch of thermal expansion parameters amount to 4.1% and 123%, respectively. The polar character of GaAs results in the formation of antiphase domains (APDs) when it is grown on exactly oriented Si(001) because of the different surface step height of the two materials [9, 20]. In order to avoid the nucleation of APDs we used mis-cut substrates known to form double layer steps [21].

Though our GaAs/Si deposits have been successfully grown crack-free and without any wafer bowing they nevertheless still exhibited crystal defects due to the lattice mismatch and polarity of the III–V deposit despite the use of offcut Si substrates. In this paper we present a transmission electron microscopy (TEM) investigation of the type and arrangement of crystallographic extended defects in GaAs microcrystals grown on Si pillars.

## 2. Experimental

The GaAs was grown on (001) Si substrates 6° off to [110] at 580°C by molecular beam epitaxy (MBE) at a rate of 0.5 ML/s with V/III = 20. The beam orientation was set at 30° off the normal to the rotating substrate. Prior to growth the Si substrate was patterned by deep reactive ion etching (DRIE), based on

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the Bosch process [22], into square-based pillars, 8  $\mu\text{m}$  high and 5 or 9  $\mu\text{m}$  wide, with various trench widths. The Si substrates were cleaned with standard RCA and finally dipped into HF. *In situ* thermal etching was done at 780  $^{\circ}\text{C}$  before GaAs deposition. The GaAs deposits investigated here were 2  $\mu\text{m}$  high on  $5 \times 5 \mu\text{m}^2$  wide pillars. Defect analysis was performed on cross-section specimens by TEM at 200 keV (STEM/TEM JEOL 2200 FS) operated in the two beam diffraction contrast, high resolution (HR-TEM) and high angle annular dark field (HAADF) modes. Strain maps to locate the dislocations at the interface were obtained by geometric phase analysis (GPA) [23, 24] processing of HR-TEM images using the STEM-CELL software package [25, 26]. The  $\langle 110 \rangle$  cross-section specimens were prepared by sandwiching a piece of the sample between two slabs of Si, followed by mechanical grinding down to 30  $\mu\text{m}$ . Thinning to electron transparency was finished by Ar ion bombardment.

### 3. Results and discussion

The GaAs microcrystals on the Si pillars had a top surface defined by  $\{113\}$  and  $\{111\}$  facets in the central and very periphery part, respectively. A scanning electron microscopy (SEM) overview is given in Fig. 1a while Fig. 1b is the STEM-HAADF image of a pillar, clearly showing the (bright) AlGaAs layers which were introduced during the growth as markers to follow the growth mechanisms. The latter ones are discussed elsewhere [27]. No crack was ever observed.

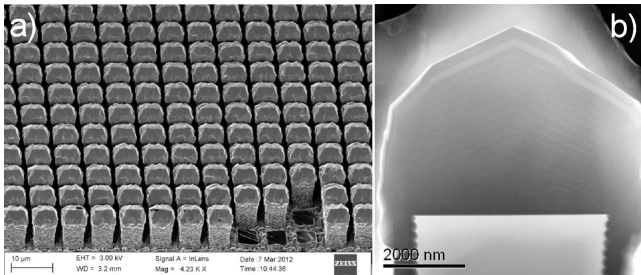


Fig. 1. (a) SEM bird's-eye view of 2  $\mu\text{m}$  thick GaAs crystals deposited on patterned Si substrate with  $5 \times 5 \mu\text{m}^2$  wide pillars, 8  $\mu\text{m}$  deep. (b) STEM-HAADF of a GaAs/Si pillar. The bright stripes are AlGaAs layers (see text).

Three main types of crystal defects have been detected, i.e., misfit and threading dislocations and stacking defects, like twins and stacking faults. Figure 2 is a TEM image in the diffraction contrast mode showing that the majority of the defects are confined to the bottom part of the GaAs deposit. Only one threading dislocation and rare twins still reach the top GaAs surface for such a limited microcrystal aspect ratio. The confinement of the threading dislocations to the lower part of the microcrystal is more efficient along its central axis. Here, the great majority of them propagate up to only a maximum

distance from the interface of about 500 nm, because of their mutual annihilation or expulsion at the deposit sidewalls. The latter mechanism prevails for those defects situated closer to the sidewalls. So-called growth dislocations oriented along  $[001]$  ([19, 28]) have not been detected.

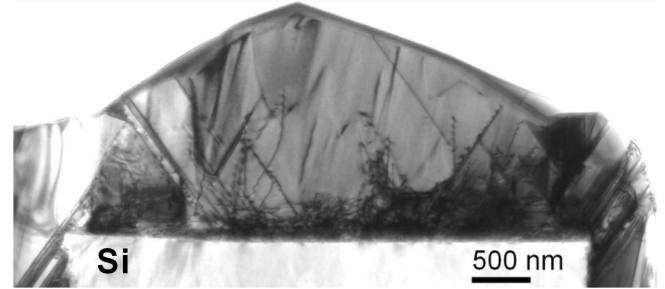


Fig. 2. TEM image of the top part of a GaAs/Si pillar showing distribution of the crystal defects in GaAs.  $g = [220]$ .

Misfit dislocations at the GaAs/Si interface, caused by the 4.1% lattice mismatch  $\varepsilon = (a_f - a_s)/a_s$  with  $a_f$  and  $a_s$  the lattice constant of the film and substrate, respectively, have been detected in cross-sectional low magnification TEM images in the two-beam contrast mode (not shown here) and in GPA maps (Fig. 3). Their average distance  $d$  is  $\approx 5$  nm, in good agreement with the expected value of 4.81 nm calculated from the formula  $d = kb/\varepsilon$ , with  $b$  — the Burgers vector value and  $k$  — a constant equal to 0.5 for  $60^\circ$  MDs and 1 for edge MDs [28]. The value of  $k = 0.5$  is due to the fact that only the edge component of a  $60^\circ$  dislocation in the growth plane relieves the strain. The mentioned measured distance  $d$  suggests that the strain was mainly relaxed by  $1/2\langle 101 \rangle 60^\circ$  type. However, as seen in the HR-TEM image of Fig. 4, also  $1/2\langle 110 \rangle$  edge MDs with  $b$  in the interface plane exist, somewhat irregularly spaced with respect to the  $1/2\langle 101 \rangle 60^\circ$  MDs. The presence of  $60^\circ$ - and  $90^\circ$ -type misfit dislocations might be consistent with the use of conditions which promote two-dimensional growth since the misfit would be relieved by the introduction of  $60^\circ$  dislocations as half loops at the deposit surface which glide to the interface on  $\{111\}$  planes [29, 30]. Under these circumstances, the edge  $90^\circ$  dislocations could be produced when two  $60^\circ$  dislocations moving on opposed  $\{111\}$  planes meet at or near the interface by a reaction of the type  $1/2 [101] + 1/2 [01\bar{1}] \rightarrow 1/2 [110]$ . The glissile  $60^\circ$  dislocations can move through the crystal by glide on  $\{111\}$  planes, which cross the whole layer from the interface to the top surface, and can thus be the sources of the threading dislocations [31].

The annihilation of the threading dislocations, hence their density reduction, can occur in several ways. Two threading dislocations on the same slip plane can combine and completely annihilate each other provided their Burgers vectors are equal and opposite according to a reaction of the type [32, 33]:  $1/2 [101] + 1/2 [10\bar{1}] \rightarrow 0$ .

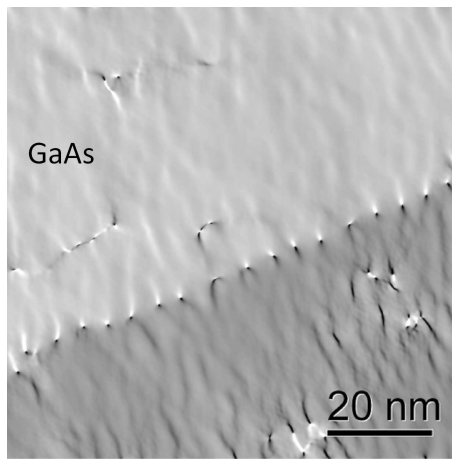


Fig. 3. Strain map obtained by GPA evidencing misfit dislocation at the GaAs/Si interface.

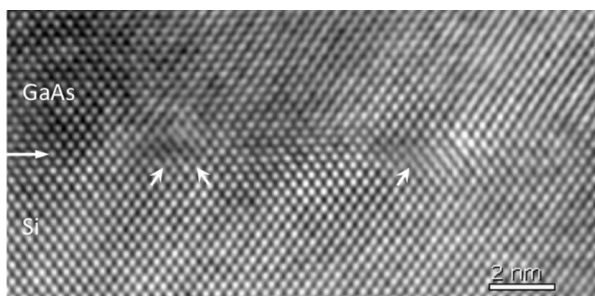


Fig. 4. HR-TEM image in  $\langle 110 \rangle$  projection of the GaAs/Si interface (indicated by the horizontal white arrow) showing two misfit dislocations. The white arrowheads inclined on  $\{111\}$  planes indicate the extra  $\{111\}$  planes of the dislocations. The dislocation on the right is a  $60^\circ$  one as it exhibits only one inserted plane. The one on the left side is a Lomer edge dislocation since it has two inserted planes, i.e. it is the interaction of two  $60^\circ$  dislocations on intersecting  $\{111\}$  planes.

The  $60^\circ$  threading dislocations can reduce their density via three other reactions, all leading to a decrease in energy. Interaction between two dislocations may in fact result in either (a) formation of dislocation loops, (b) one  $1/2[110]$  type dislocation [32, 33] or (c) formation of a faulted pair.

The formation of loops requires the formation and development of a dislocation dipole by the interaction of dislocations lying on parallel glide planes. The loops are generated when the dipole breaks up because of the mutual attraction of the negative and positive arms of the dipole which produces a row of dislocation loops [34]. The dislocation loops indicated by arrows in Fig. 5 should have formed by shrinkage of dislocation dipoles suggesting that also this mechanism played a role in the dislocation density reduction. The absence of the rows of loops can be due to the removal of the loops other than the visible ones during the preparation, i.e. thinning, of

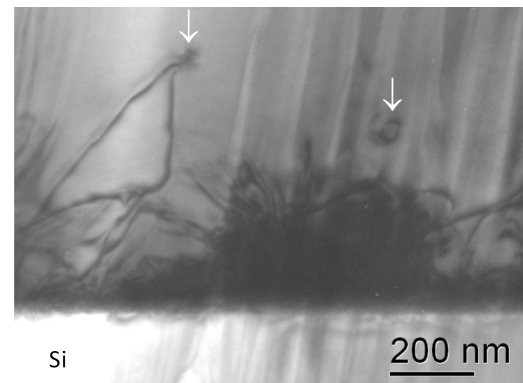
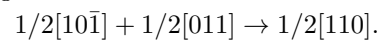


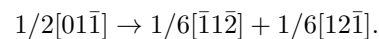
Fig. 5. TEM image in the two beam diffraction contrast mode ( $g = \langle 400 \rangle$ ) of threading dislocations close to the interface and dislocation loops (arrowed).

the TEM specimen. Threading dislocation annihilation with formation of loops has been reported by several authors [32, 35].

The interactions of type (b) between two threading dislocations in the layer gliding on the  $(111)$  and  $(\bar{1}\bar{1}1)$  planes with Burgers vectors  $1/2[10\bar{1}]$  and  $1/2[011]$ , respectively, can be described by a reaction like the following:



The dislocation on the right is an edge one, hence sessile, and cannot move further as well. The faulted pairs (reaction (c)) occur by dissociation of  $60^\circ$  threading dislocations to produce two Shockley partials according to



In so doing a stacking fault ribbon between the Shockleys is formed. In the case of a  $60^\circ$  dislocation the two Shockleys are of the  $90^\circ$  and  $30^\circ$  type with their  $\mathbf{b}$  making a  $90^\circ$  and  $30^\circ$  angle, respectively, to the dislocation line. The dissociation can take place when the leading partial is faster than the trailing one. Under compressive stress conditions, like for GaAs/Si, the first nucleated partial, i.e. the leading partial, is the  $30^\circ$  one, while the  $90^\circ$  one is nucleated afterwards and is the trailing one [36]. The velocity of the  $30^\circ$  partial is smaller than the one of the  $90^\circ$  partial [36–38]. Dislocations in compressive layers will thus have negligible dissociation, if any, because the greater velocity of the trailing  $90^\circ$  will make it to instantly follow the  $30^\circ$  partial after its nucleation.

The stacking defects were mostly twins of various width while stacking faults were rarely seen. An image of twins is shown in Fig. 6a. The twin nature of these defects is confirmed by the electron diffraction pattern taken from them (Fig. 6b) that shows the presence of two weak extra spots repeated along the two  $\langle 111 \rangle$  directions of the reciprocal lattice spaced  $1/3$  of the  $\{111\}$  plane spacing, typical of the twins [39]. The strongest spot of the two extra spots is a twin spot while the weakest one is attributed to double diffraction [39]. The twins, too,

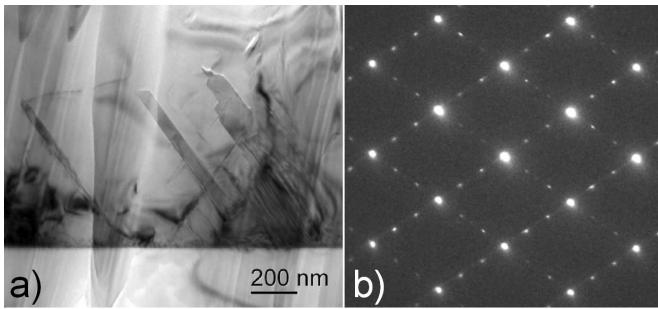


Fig. 6. (a) TEM image in the two beam diffraction contrast mode ( $g = \langle 400 \rangle$ ) of twins. (b) Electron diffraction pattern from the twin region in (a).

can reduce their propagation to the top of the deposit by mutual interaction as the epilayer becomes thicker and thicker.

The generation of the twins may have occurred in several ways, e.g. by mis-deposition of arriving atoms on the  $\{111\}$  facets of growth nuclei that form in the very early growth stages [40, 41]. Following the usual ABCBCA notation to denote the stacking sequence of the  $\{111\}$  planes let us take as reference plane the one occupied by the A sites. For correct stacking, atoms in the next plane need to occupy the B sites. When a stacking error occurs, however, the atoms will occupy the C sites and the sequence will become ABCA|C. The next layer of atoms will determine the fault type. If the atoms deposit on the A sites, and continue growing in the correct sequence, the result will be ABCA|CABC and an intrinsic stacking fault would form. If the atoms deposit instead on the B sites, and then continue the correct deposition, the result will be an extrinsic fault with a stacking sequence ABCA|C|BCA. However, if the atoms deposit on the B sites and continue the deposition in the inverse sequence, a twin will result with the stacking sequence ABCA|CBAC. In contrast to  $\{111\}$  surfaces, the energy of the correct atomic sites on  $\{001\}$  surfaces is significantly lower than the energy on any other site, i.e. deposition errors on  $\{001\}$  surfaces are very unlikely. Therefore, once a continuous flat  $\{001\}$  epilayer forms by coalescence of the nuclei further growth takes place in the two-dimensional mode and the formation of new planar defects should stop. However, existing planar defects will keep on growing unless they intersect each another or anti-phase boundaries. The effectiveness of this mechanism for twin generation should not be negligible as the MBE growth should occur in a three-dimensional mode, i.e., with formation of growth nuclei [42].

A second generation source of the twins can be the steps associated with the mis-orientation of the substrate [30, 43, 44]. In particular, Wei and Aindow calculated the resolved shear stress for the possible twinning systems in GaAs/Si and found that such shear stress increases in vicinal substrates with respect to nominal ones. They thus suggested that the twins present in layers grown on

vicinal substrates are actually deformation twins which arise in response to that part of the misfit strain which is not accommodated by misfit dislocations [30]. It should be noted that twins can really relax strain through the edge component in the interface plane of the Shockley partials bordering them. It is believed that both mechanisms have been effective to produce the twins.

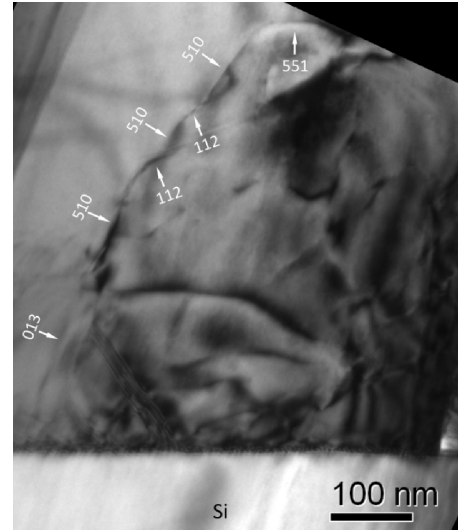


Fig. 7. TEM image of the GaAs/Si interface. The continuous bending of the long defect extending from the interface to the top of the picture with changing of the crystallographic planes on which it lies, as indicated, suggests that it is an antiphase boundary.  $g = \langle 220 \rangle$ .

The zig-zag like continuous bending of the long defect of Fig. 7 extending from the interface to the top of the picture and its lying on different crystallographic planes such as (112), (013), (510) and (551), which is the behavior of antiphase domain boundaries [20, 45], suggests that it is an antiphase boundary. It seems to bend over back to the interface indicating that very likely it could have undergone annihilation without reaching the top surface. This was the only antiphase boundary observed suggesting that growth on offcut substrate was effective to prevent their formation.

#### 4. Conclusions

Growth of 2  $\mu\text{m}$  thick GaAs microcrystals on square-shaped pillars with size of some  $\mu\text{m}$ , obtained by patterning of misoriented (001) Si substrate, was effective to avoid the formation of cracks and bowing in the GaAs that typically form in thick III-V continuous layers on Si. The offcut of the pillars drastically limited the density of antiphase domain boundaries. Because of the lattice mismatch other extended defects potentially harmful for device operation, i.e. threading dislocations and twins, were also present. However, the threading dislocations were practically all confined to the bottom part of the GaAs microcrystal, i.e. quite far from any active region

that would be established by growing any other III–V compound on the GaAs. Twins as well are confined in the bulk of the microcrystal and only very seldom reach the topmost surface. However, due to their lack of dangling bonds twins are not expected to be electrically active. Hence, they should not be detrimental for device operation. Only intersecting twins can give rise to unsatisfied bonds [44] but such twin structures have not been observed at the GaAs top.

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