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Analysis of Signals Pre-processing Algorithm in Case of Hardware and Software Implementation on Diagnostic Programmable Device PUD-2

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In the paper, two-stage signal pre-processing algorithm based on the filtration is presented. The developed algorithm is dedicated for the diagnostic programmable device PUD-2. The PUD-2 is the real-time analyzer based on programmable logic devices FPGA, as well as on ARM processor. Application of FPGA programmable devices and ARM processors allows to merge advantages of hardware and software implementations. Further, analysis of digital filters parameters in case of its efficient realization on the FPGA is presented. The aim of the study is to select digital-filter parameters in such way that the available resources of FPGA are used efficiently and filter characteristics meet established criteria. In the study, low pass finite impulse response and infinite impulse response filters are compared. For the first stage of the signal pre-processing algorithm, hardware implementation of the infinite impulse response filter is proposed, contrary to the second stage, where software realization of the finite impulse response filter is suggested. Combination of hardware and software filtration algorithms allows for fast and efficient realization of signal pre-processing algorithm used in analysis carried out on the PUD-2.

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1. Introduction

In the paper, analysis of digital filters parameters in case of its efficient realization on the diagnostic programmable device PUD-2 is presented. The PUD-2 is a real-time analyzer, and its architecture allows for hardware realization of signal pre-processing algorithms. Processing unit of the device consists of field programmable gate array (FPGA) Spartan-3 and advanced RISC machine processors (ARM) Cortex-A8. Such architecture allows to merge advantages of a hardware (FPGA) and a software (ARM) implementation. The PUD-2 is divided into two modules: a digital module and independent analog-to-digital converters.

In the acquisition process on the PUD-2, samples are provided by analog-to-digital converters [1] directly to the FPGA. Signal pre-processing is carried out on the FPGA. Such implementation requires fixed-point representation of the data. Beside of the benefits such as parallelism of computations, reliability, and performance of such implementation, the hardware realization has certain disadvantages, including timing parameters and fixed-point notation [2, 3]. The fixed-point notation of filter coefficients can affect its frequency response [4]. The larger word length value, the less the fixed-point representation distorts the filter parameters. However, a larger word length value also requires more hardware resources, so it is important to specify a word length that provides an acceptable tradeoff between distortion and hardware resource consumption. This problem was raised by the authors in [5–8]. The filtration on the PUD-2 is realized by a specialized module implemented on the FPGA device and the ARM processor. In the study, two types of digital filters are discussed, an infinite impulse response (IIR) and a finite impulse response (FIR).

A digital filter can be depicted as an algorithm implemented on a digital circuit. If a signal occurs at its input, a signal will arise at the output which contains of certain range of frequencies, in the frequency range called pass-band of the filter, while other frequencies will be dumped (stop-band). Every digital filter can be depicted by responses to an impulse, a step, and frequency. During design of filters, the specified frequency requirements are assumed. For this purpose, the frequency response of the filter is designed [9]. The equations describing frequency response of digital filter can be written in the form

$$Y(\Omega) = |H(\exp(\mathrm{i}\,\Omega))|\,, \tag{1}$$

$$\Omega = \frac{2\pi f_t}{f_s}, \quad \Omega \in [-\pi, \pi], \tag{2}$$

where $Y(\Omega)$ is a frequency response function of filter $H(\exp(\mathrm{i}\,\Omega))$, Ω is a ripple, f_t is a cut-off frequency, and f_s is a sampling frequency. In the study a low pass filter has been analyzed. Its frequency response functions can be described by

$$|H_{LP}(\exp(\mathrm{i}\,\Omega))| = \begin{cases} 1 \pm \delta_{\text{pass}} & \text{for } |\Omega| \leq \Omega_{\text{pass}} \\ 0 \pm \delta_{\text{stop}} & \text{for } |\Omega| \geq \Omega_{\text{stop}} \end{cases}, \tag{3}$$

where δ_{pass} is a ripple in pass band and δ_{stop} is the ripple in a stop band.

The FIR filters are realized on the basis of convolution theorem. They are efficient in a frequency domain, but in a time domain work significantly worse. The most important feature of the FIR filters is their stability and linear phase. The non-recursive filtration is expressed by

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$$y[n] = \sum_{m=0}^{N-1} h[m]x[n-m] = \sum_{m=0}^{N-1} b_m x[n-m], \qquad (4)$$

where y is the output signal, x is the input signal, h is the filter impulse response, b_m is the filter coefficient, N is the length of filter impulse response, and n is the length of filtered signal.

The IIR filters are realized on the basis of recursive formula, i.e. each sample of the output signal depends on the input signal and results of previous integration. The recursive formula can be written as

$$y[n] = a_0 x[n] + a_1 x[n-1] + a_2 x[n-2] + \ldots$$
$$+ b_1 y[n-1] + b_2 y[n-2] + \ldots, \qquad (5)$$

where a and b are IIR filter coefficients. The main advantage of these filters is performance but they are characterized by less accurate filtration and instability for high orders (above 20) compared to FIRs. For this reason, selection of filter type should be based on assumed criteria for filtered signal. The IIRs are characterized by non-linear phase response. This kind of filters can be unstable because of a feedback line in their structure [9].

The hardware realization of the filters on the PUD-2 device is provided by specialized module implemented on the FPGA. This module allows to realize filters with maximum order up to 29. Module act as interface between an analog-to-digital converters and a bus. It allows to register signals with sampling frequency up to 1 MHz. In the paper, two stage signal pre-processing algorithm based on filtration is proposed.

2. Digital filters analysis in case of hardware and software implementation

2.1. Criteria for the analyzed filters

The aim of the study presented in this chapter is to select digital-filter parameters in such way that the available resources of a FPGA are used efficiently and filters characteristics meet established criteria for a fixed-point implementation. Firstly, some definitions have to be given. A word length indicates the number of bits used to represent a fixed-point number, while an integer word length specifies the number of bits, including the sign bit used in representation of an integer part of a fixed-point number. The difference in bits between a word length and an integer word length determines digits of precision. The value of a signed fixed-point number is defined by

$$Q[x] = 2^n \left(-2^{-1} b_1 + \sum_{k=2}^{m} 2^{-k} b_k \right), \qquad (6)$$

where b_k is a binary digit, n is the integer word length, and m is the word length. The highest representable number can be expressed by $2^n(2^{-1}-2^{-m})$ and the lowest representable number is 2^{n-1}. In the study, the nearest rounding mode and saturation overflow mode has been used. As presented in the paper [8], for filters coefficients the integer word length cannot be modified because it results in large distortion of its characteristics.

In the study, a low pass FIR and an IIR filters have been compared. The effect of a coefficients word length on the filter characteristics are presented. For the implementation of the digital filters on the Field Programmable Gate Array, accuracy of the filters is limited by the finite word length. When a filter is constructed with digital hardware, the minimum word length for the specified performance must be determined. An ideal filter requires infinite word length for real representation of the filter coefficients [10, 11]. In this study, an integer word length is written with a number of digits not changing it accuracy e.g. the one of the coefficients of the Chebyshev II filter is 3.168665429473, the integer word length is 3 so 2 bits for this number have to be used and the number after radix point is 168665429473 with assumed accuracy of 10 digits of precision one obtains a number with lower accuracy which is 1680. In the study, the effect of digits of precision of the coefficients on the filters characteristics are presented. To implement a digital filter, firstly criteria for its magnitude response have to be established. In Fig. 1, the frequency response of a low-pass filter with assumed 'tunnel' is presented.

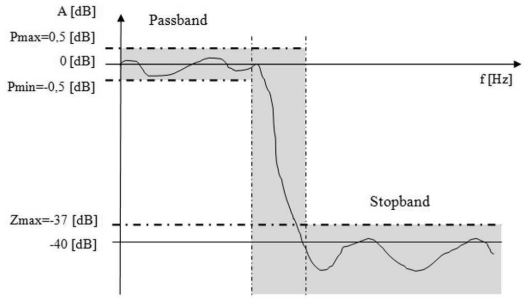

Fig. 1. The frequency response of a low-pass filter.

The criteria for analyzed filters are as follows: $P_{\max}$ — maximum ripple in the passband and in the transient band should be lower than 0.5 dB, $P_{\min}$ — minimum ripple in the passband should be higher than –0.5 dB, $Z_{\max}$ — maximum ripple in the stopband should be lower than –37 dB.

2.2. Analysis of the filters parameters

The analysis have been conducted for particular filters, the Inverse Chebysev filter (of order 8) and the FIR filter designed by the window method (of order 100). These two types have been chosen on the basis of the previous study [8]. The analysis have been conducted for different normalized cut-off frequencies. In Tables I and II, results of investigated parameters of filters characteristics are presented.

The following parameters of the frequency response of the filters were investigated; the maximum ripple in the pass band and in the transient band ($P_{\max}$), the minimum ripple in the pass band ($P_{\min}$), and the maximum ripple in the stop band ($Z_{\max}$). The parameters were presented according to digits of precision for coefficients. The minimum investigated number of digits of precision

TABLE I
Parameters of 8-order type II Chebyschev filter.

f_c	parameter	Digits of precision						
	[dB]	4	6	8	10	12	14	16
0.2	$P_{\max}$	*35*	*5*	*20*	*20*	0	0	0
	$P_{\min}$	*−5*	*−40*	*3*	*−2*	0	0	0
	$Z_{\max}$	*−10*	*5*	*0*	*−10*	−38	−38	−40
0.3	$P_{\max}$	*8*	*0*	*5*	*0*	0	0	0
	$P_{\min}$	*−4*	*−4*	*−1*	*0*	0	0	0
	$Z_{\max}$	*−10*	*−17*	*−17*	*−32*	−38	−39	−39
0.4	$P_{\max}$	*15*	*−3*	*0*	*0*	0	0	0
	$P_{\min}$	*−5*	*−4*	*−1*	*0*	0	0	0
	$Z_{\max}$	*−5*	*−33*	*−37*	*−35*	−40	−40	−40
0.5	$P_{\max}$	*1*	*0*	*0*	0	0	0	0
	$P_{\min}$	*−1*	*0*	*0*	0	0	0	0
	$Z_{\max}$	*−5*	*−20*	*−33*	−38	−40	−40	−40
0.6	$P_{\max}$	*1*	*0*	*0*	0	0	0	0
	$P_{\min}$	*−1*	*0*	*0*	0	0	0	0
	$Z_{\max}$	*−4*	*−20*	*−35*	−37	−40	−40	−40
0.7	$P_{\max}$	*40*	*1*	*1*	*0*	*0*	0	0
	$P_{\min}$	*−6*	*−1*	*−1*	*0*	*0*	0	0
	$Z_{\max}$	*8*	*−3*	*−18*	*−30*	*−35*	−38	−40
0.8	$P_{\max}$	*1*	*37*	*11*	*1*	*0*	*0*	0
	$P_{\min}$	*−35*	*−3*	*0*	*−1*	*0*	*0*	0
	$Z_{\max}$	*35*	*4*	*13*	*−8*	*−24*	*−33*	−38

TABLE II
Parameters of 100-order FIR filter.

f_c	parameter	Digits of precision						
	[dB]	4	6	8	10	12	14	16
0.2	$P_{\max}$	*−1*	*1*	0	0	0	0	0
	$P_{\min}$	*−5*	*−3*	0	0	0	0	0
	$Z_{\max}$	*−10*	*−24*	−37	−38	−43	−43	−43
0.3	$P_{\max}$	*−1*	*0*	*0*	0	0	0	0
	$P_{\min}$	*−6*	*−3*	*0*	0	0	0	0
	$Z_{\max}$	*−10*	*−23*	*−32*	−42	−43	−43	−43
0.4	$P_{\max}$	*−2*	*0*	*0*	*0*	0	0	0
	$P_{\min}$	*−5*	*−3*	*0*	*0*	0	0	0
	$Z_{\max}$	*−13*	*−27*	*−33*	*−35*	−41	−46	−46
0.5	$P_{\max}$	*0*	*1*	*0*	0	0	0	0
	$P_{\min}$	*−4*	*−3*	*0*	0	0	0	0
	$Z_{\max}$	*−10*	*−20*	*−34*	−42	−43	−43	−43
0.6	$P_{\max}$	*0*	*1*	*0*	0	0	0	0
	$P_{\min}$	*2*	*−2*	*0*	0	0	0	0
	$Z_{\max}$	*−5*	*−23*	*−32*	−43	−43	−43	−43
0.7	$P_{\max}$	*1*	*0*	*0*	0	0	0	0
	$P_{\min}$	*−2*	*−3*	*0*	0	0	0	0
	$Z_{\max}$	*−3*	*−27*	*−33*	−44	−44	−44	−44
0.8	$P_{\max}$	*0*	*1*	0	0	0	0	0
	$P_{\min}$	*−2*	*−2*	0	0	0	0	0
	$Z_{\max}$	*−12*	*−27*	−37	−45	−45	−45	−45

was 4 and the maximum 16. In Tables I and II values marked with italics represent filters which do not meet the criteria presented in Fig. 1. In Fig. 2, the IIR filter parameters versus the number of digits of precision are presented.

Fig. 2 presents parameters for the Inverse Chebyshev filter (of order 8) with normalized cut-off frequency 0.2. For this filter, the investigated parameters were changing significantly up to 8 bits, the maximum ripple in the stop band stabilize on (–40 dB) for 12 bits. In Fig. 3, the FIR filter parameters versus the number of digits of precision are presented.

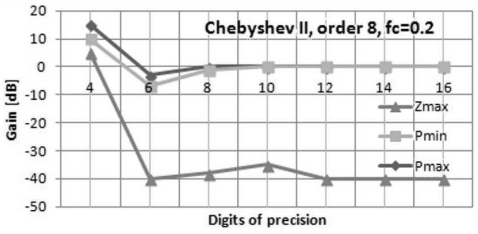

Fig. 2. The IIR filter parameters versus the number of digits of precision.

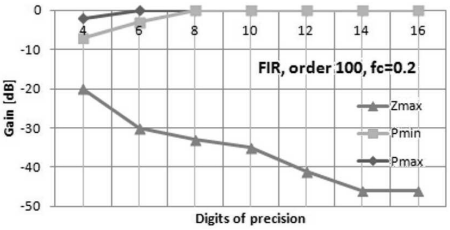

Fig. 3. The FIR filter parameters versus the number of digits of precision.

For the IIR filter, the same as for the FIR the parameters $P_{\min}$ and $P_{\max}$ reach expected value (0 dB) for 8 bits. The parameter $Z_{\max}$ was decreasing rapidly from 4 bits to 14 bits. On the basis of presented results it can be stated that the digital filter characteristics for fixed-point notation strongly depend on number of digits of precision.

2.3. Implementation of the digital filters

Purpose of this study is to implement digital filters on the Diagnostic Programmable Device. The PUD-2 device is based on programmable logic device FPGA and ARM processor. Device allows for software and hardware realization of a signal pre-processing algorithm. In case of hardware realization of the filters, computation is very fast but their characteristics strongly depend on word length for fixed-point notation. In case of software realization, filtration is more accurate but computation time is longer.

On the basis of results presented in previous section, only one analyzed IIR filter meets assumed criteria in all range of cut-off frequencies. It requires 16 digits of precision for its coefficient, while there are three FIR filters (12, 14 and 16 digits of precision). In Fig. 4, the analyzed FIR and IIR filter magnitude responses for cut-off frequency 0.2 and 4 digits of precision are presented.

In the case presented in Fig. 4 for fixed-point notation (dotted line) the word length (4 digits of precision) was

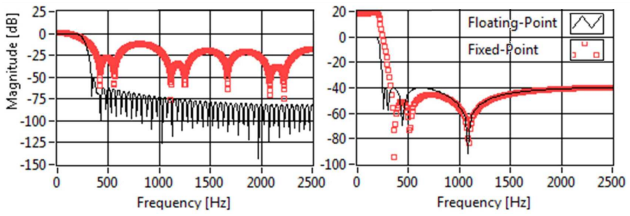

Fig. 4. Magnitude response for $f_c = 0.2$ and 4 digits of precision: (left) FIR, order 100; (right) Chebyshev II, order 8.

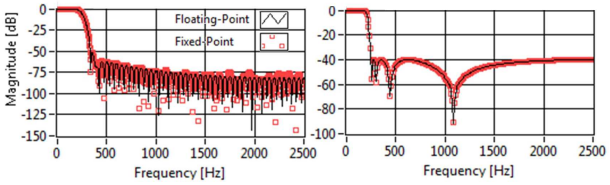

Fig. 5. Magnitude response for $f_c = 0.2$ and 16 digits of precision; (left) FIR, order 100; (right) Chebyshev II, order 8.

insufficient to model original frequency response of the filters (solid line). Other case was presented in Fig. 5 where filter characteristics for 16 digits of precision are presented. In this case both plots overlap.

In the example shown in Fig. 5, the phenomenon connected with fixed-point notation of filters' coefficients is presented. Two kinds of filters were studied, FIR and IIR. For both filters the effect of the cut-off frequency on required number of digits of precision can be noticed.

The hardware implementation of the filter on the PUD-2 device is realized by a specialized module implemented on the FPGA device. This module allows to realize filters with order of up to a maximum of 29. The sampling frequency of the analog-to-digital converters of the PUD-2 device is 1 MHz. For signal filtration to low frequency range, two-stage signal filtration algorithm is proposed. For the first stage, hardware implementation of the Chebyshev filter (type II, order 8) with 16 digits of precision for the coefficients is proposed. For the second stage, software FIR filter realized by the ARM processor is suggested. Software implementation of this filter allows the user to set up an arbitrary cut-off frequency. The combination of the hardware and the software filtration algorithms enables fast and efficient realization of the signal pre-processing algorithm on the PUD-2 device.

3. Summary

In the paper, analysis of digital filters in case of implementation on the programmable device PUD-2 is presented. In the study, the low pass FIR and IIR filters have been compared. The most important advantage of the FIRs are stability and linear phase; on the other hand, IIRs are more efficient. Benefits of implementation of the filters on the Field Programmable Gate Array are parallelism of computations, reliability, and performance, but such implementation requires specifies timing parameters and fixed-point notation. The fixed-point notation of filter coefficients affects its parameters. It is important to specify a word length that provides an acceptable trade-off between distortion and hardware resource consumption. In the study, one IIR filter (16 digits of precision) and three FIR filters (12, 14, 16 digits of precision) fulfill assumed criteria in the whole analyzed cut-off frequencies range. The two-stage signal pre-processing algorithm for the PUD-2 device was proposed. For the first stage, hardware implementation of the Chebyshev filter (type II, order 8), and for the second stage software realization FIR filter are proposed. Combination of hardware- and software-based filtration algorithms enable fast and efficient realization of signal pre-processing algorithm used in analysis carried out on the PUD-2.

Acknowledgments

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