Proceedings of the IX International Conference ION 2012, Kazimierz Dolny, Poland, June 25–28, 2012

Superconducting Layers by Gallium Implantation and Short-Term Annealing in Semiconductors

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Superconducting layers in silicon and germanium are fabricated via gallium implantation through a thin SiO_2 cover layer and subsequent rapid thermal annealing. Gallium accumulation at the SiO_2/Si and SiO_2/Ge interfaces is observed but no pure gallium phases were found. In both cases superconducting transition occurs around 6–7 K which can be attributed to the metallic conducting, gallium rich interface layer. However, the superconducting as well as the normal-state transport properties in gallium overdoped silicon or germanium are different.

DOI: 10.12693/APhysPolA.123.916

PACS: 74.78.−w

1. Introduction

Since the recent discovery of superconductivity in diamond, the interest in superconducting group-IV semiconductors has been renewed [1]. Boron doped diamond, fabricated via high-pressure high-temperature synthesis (HPHT) and chemical vapour deposition (CVD), reached critical temperatures of $T_C = 7$ K [2, 3]. Surprisingly, also the technologically more relevant semiconductors silicon [4] and germanium [5–7] line up in this interesting group of materials. The key for superconductivity in doped semiconductors is the activation of charge carrier densities above the metal–insulator transition (MIT) [8]. Increasing carrier densities are often limited by the equilibrium solid solubility and therefore, dopant precipitation has to be prevented [9, 10]. This threshold can be overcome by using nonequilibrium doping techniques like gas immersion laser doping [4, 11] or ion implantation with subsequent short-term annealing [12]. The first was used to fabricate superconducting B doped Si with critical temperatures of 0.6 K [11, 13]. Gallium is a promising acceptor in Ge allowing for high doping levels [14]. Indeed, superconductivity has been found in Ga doped Ge fabricated via ion implantation and short-term annealing [5–7]. This is the only method that is fully compatible with standard microelectronic technology and therefore this process might be used for new superconducting microelectronics [15].

Critical temperatures up to 1 K were achieved in Ga doped Ge, but the high doping levels of several at.% imply the question if the superconductivity can be attributed to a doping effect or originates from cluster formation [16]. Intense structural investigations of the superconducting layers clearly exclude Ga clusters with a size of more than 3 nm [12]. As Ga itself is a superconducting element with various superconducting phases showing critical temperatures between 1 K and 12 K [17], the question has to be addressed, how superconducting precipitates influence the low temperature transport properties. A high fluence Ga implantation in Si can be used for this task because of the low equilibrium solid solubility of 0.1 at.% [18], leading to Ga precipitation [19–21].

2. Experimental

We used standard microelectronic Czochralski-grown n-type Si and Ge wafers with (100) orientation as substrates. To protect the surface during ion implantation and prevent out-diffusion while annealing, a 30 nm SiO_2 cover layer was sputter deposited on top. According to the Rutherford-backscattering spectrometry (RBS), the implantation of 4×10^{16} cm^{-2} Ga ions at 80 keV in Si and 100 keV in Ge leads to Gaussian like implantation profiles with a full width at half maximum of 40 nm. The peak concentration of 11 at.% in Si (13 at.% Ge) is located 30 nm beneath the SiO_2/Si (SiO_2/Ge) interface [22–24]. During the implantation at room temperature a roughly 90 nm thick amorphous layer is formed. The wafers were cut into pieces of 1×1 cm^2 and subjected to a 60 s rapid thermal annealing (RTA) in flowing argon atmosphere to recrystallize the implanted layer. For the Si layers, RTA temperatures ranging from 550 °C to 750 °C were used. In the former investigation we found superconductivity in Ga doped Ge after RTA processing at temperatures between 850 °C and 910 °C [6]. Therefore, the present experiments use equal annealing conditions.

3. Results and discussion

In order to investigate the Ga distribution in the SiO_2/Si layer stack after annealing, RBS with a 1.2 MeV

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He^+ beam was used. Thereby a polycrystalline layer structure and a strong Ga redistribution towards the SiO_2/Si interface (see Fig. 1) is observed, forming a 10 nm thin nanolayer with a Ga concentration of up to 20 at.%. In the deeper region, between 45 and 80 nm, a plateau like Ga concentration of 5 at.% remains, creating in this way a heavily Ga doped layer with a long range tail in the Si substrate. Energy filtered transmission electron microscopy (EFTEM) is used to investigate the Ga distribution in more detail as the RBS profile is averaged laterally over 1 mm^2. The Si L absorption edge around 99 eV is a suitable energy for an indirect detection of the Ga distribution. One representative cross-section result of a sample annealed at 700 °C is shown in the pseudocolor image (Fig. 1). Only 20 nm of the SiO_2 cover layer remain after implantation due to sputtering. The depletion of Si at the SiO_2/Si interface due to Ga accumulation and O intermixing during implantation is clearly indicated. However, no pure Ga clusters, but amorphous precipitates consisting of a mixture of Ga, Si and O were found. Similar investigations on the layers annealed at different temperatures and times show the same microstructure and Ga distribution [22, 23, 25].

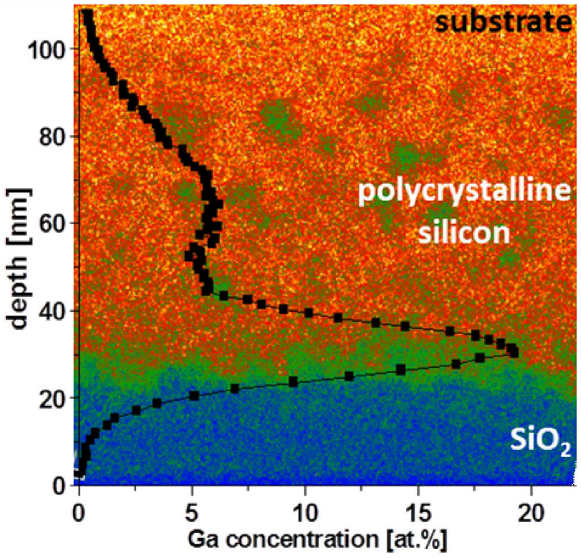

Fig. 1. Cross-section EFTEM pseudocolor image of the Si distribution in a layer annealed for 60 s at 700 °C. Orange corresponds to a high and blue to a low Si concentration. The average Ga depth distribution as measured by RBS is overlaid.

The sheet resistance as a function of temperature (shown in Fig. 2) was investigated by electrical transport measurements in van der Pauw geometry [26]. This data can be interpreted only when the multilayer structure of the samples is considered. At high temperatures most of the measurement current flows through the substrate and influences the result. Below 20 K the substrate and the Ga tail region become insulating because the charge carriers freeze out. Therefore, at low temperatures, only the highly Ga doped Si and Ga rich interface layer contribute to the signal. With increasing RTA temperature from 550 °C to 700 °C, the sheet resistance in the normal-state (e.g. at 10 K) systematically decreases from 9 kΩ/sq to 1 kΩ/sq. After annealing at 750 °C it increases to 7.5 kΩ/sq. In a narrow annealing temperature window between 600 °C and 700 °C a transition into a superconducting state around 6–7 K occurs. These critical temperatures are comparable to those found for amorphous Ga films, although we have definitely no amorphous Ga layer in our samples [16, 27]. If the SiO_2 cover layer and the Ga rich interface layer are removed by diluted HF, the superconductivity vanishes and the normal state sheet resistance increases to a value comparable to the non-superconducting layers [23]. This proves that the superconducting state appears in the Ga rich interface layer. The normal-state transport properties of the superconducting samples (RTA at 600–700 °C) are also dominated by this Ga rich interface, whereas the highly doped Si layer controls the transport in the samples, annealed at 550 and 750 °C. This explains the nonsystematic evolution of the sheet resistance with annealing temperature. Similar to thin amorphous Ga films there is a correlation of the superconducting properties and the normal state sheet resistance [25, 28]. With decreasing normal state sheet resistance the critical superconducting values increase which might be attributed to a better connected Ga rich interface layer. The lowest sheet resistance and highest critical values were found for RTA at 700 °C. If an external magnetic field is applied perpendicular to the surface, the critical magnetic field B_C is in the range of 9 T and increases to 14 T if the magnetic field points parallel to the surface. This anisotropy is typical of thin superconducting layers. Together with the critical current density $j_C \approx 2$ kA/cm^2, the critical values found in our Ga rich interface layers are competitive with Nb/Al films, commonly used for nowadays SQUID fabrication [29].

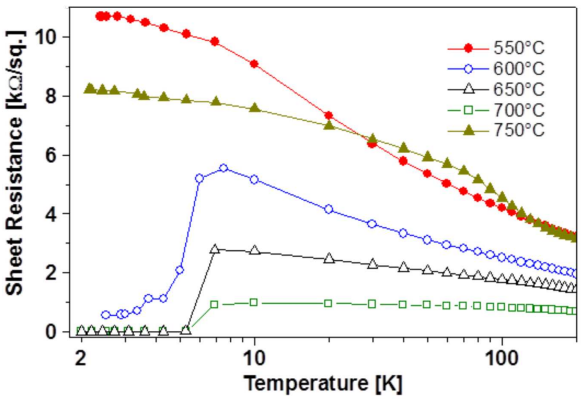

Fig. 2. Sheet resistance for the Si layers annealed for 60 s at different temperatures.

From the results presented above it is very important to notice that pure Ga phases are not necessary for superconductivity driven by Ga accumulation. Supercon-

ducting Ga rich precipitates shift the transition temperature to values comparable with amorphous Ga films. With this knowledge it is possible to prepare similar layers in Ge.

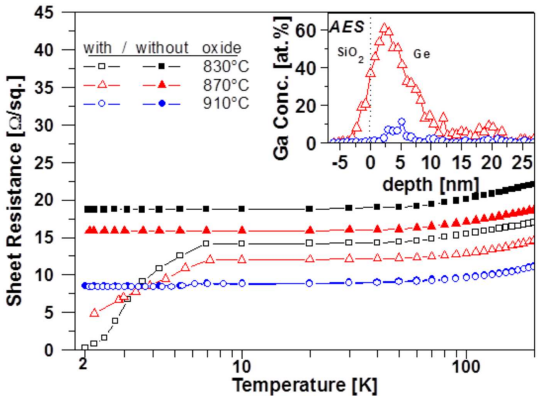

Fig. 3. Sheet resistance as function of temperature for Ga implanted Ge before and after surface etching. The inset shows the Ga concentration at the SiO_2/Ge interface measured with AES for selected samples.

Structural investigations by means of RBS and TEM reveal distinct differences of the layer structure in comparison to the Ga implanted Si because the implanted Ge recrystallizes via solid phase epitaxy [12, 24]. For the lower annealing temperatures the layer consists of single crystalline grains having a lateral size from several tens to more than 100 nm. With the increasing RTA temperature, the layers become single crystalline. A lot of efforts like TEM or time of flight secondary ion spectrometry (ToF–SIMS) have been done to localize Ga clusters in the Ge matrix [24]. Ge clusters in the SiO_2 cover layer and SiO_2 precipitates in the implanted region because of ion beam mixing could be detected. However, we did not find any hint for pure Ga. The SIMS data collected beneath the SiO_2 cover layer reveal a Ga dose loss of 77% while annealing. A Ga concentration of 3 at.% remains in the layer when taking the calculated as-implanted maximum of 13 at.% as the reference. This is well above the solid solubility limit and forms a highly Ga doped Ge layer [24]. Unfortunately, matrix effects influence the SIMS yield, which makes it difficult to determine the real Ga concentration at the SiO_2/Ge interface. This disadvantage can be overcome by the additional Auger electron spectroscopy (AES) measurements. These investigations show a Ga concentration up to 60 at.% at the SiO_2/Ge interface after annealing at 870 °C. With increasing annealing temperature, this concentration decreases to 7 at.% at 910 °C (see Fig. 3). Therefore, the Ga, missing in the deeper lying regions of the implanted layer, accumulates at the SiO_2/Ge interface and forms a Ga rich layer [24].

TABLE

Comparison of the structural, normal conducting and superconducting properties for different superconducting layer systems. The Ga rich interface layer (column 2 and 3) shows distinct differences to Ga doped Ge (column 4).

	Si:Ga [23]	Ge:Ga [6, 24]	
Ga fluence	4×10^{16} cm^{-2}	4×10^{16} cm^{-2}	2×10^{16} cm^{-2}
SiO_2 on top	yes	yes	no
RTA temperature	600–700 °C	830–870 °C	850–910 °C
microstructure	nanocrystalline	poly/single crystalline	single crystalline
R_{Sheet} at 10 K	1–6 kΩ/sq.	12–14 Ω/sq.	11–18 Ω/sq.
carrier concentration	10^{14}–10^{16} cm^{-2}	$\approx 10^{16}$ cm^{-2}	$\approx 7 \times 10^{15}$ cm^{-2}
T_C	7 K	≈ 6 K	< 1 K
transition width	< 2 K	> 5 K	< 0.4 K
B_C	9–14 T	0.5–0.8 T	< 1 T

The sheet resistance measurements shown in Fig. 3 reveal a lower normal state sheet resistance in the range of 14 Ω/sq. (830 °C) to 8.7 Ω/sq. (910 °C) compared to the Si substrate (see Table). A superconducting transition occurs around 6 K but in contrast to the sharp transition observed for Si it now has a width of around 5 K. To check whether the superconductivity is located at the Ga rich interface layer, the SiO_2 was etched with diluted HF. After surface etching the sheet resistance increases and superconductivity vanishes (see Fig. 3). As the increase of sheet resistance scales with the Ga amount at the interface it can be concluded that a high conducting layer has formed at the interface [24]. The superconducting state itself is less robust than that observed for the Ga rich nanolayers in Si. The critical magnetic fields of 0.5 T and the critical currents of several A/cm^2 are more comparable to the Ga doped Ge layers (compare Table) [5–7].

4. Conclusion

In conclusion, it could be shown that Ga rich layers can be fabricated via ion implantation of 4×10^{16} cm^{-2} Ga and stabilized at the SiO_2/Si and SiO_2/Ge interfaces by subsequent rapid thermal annealing. These layers can

become superconducting at defined annealing temperatures of 600–700 °C in Si and 830–870 °C in Ge. The superconducting nanolayers are sandwiched between the SiO_2 cover layer and the highly doped semiconducting matrix. Therefore it is challenging to investigate the isolated properties of the nanolayer. However, it can be removed by surface etching and it turns out that this superconducting interface layer dominates the normal-state transport properties, too. Although the critical temperature is comparable, the superconducting properties differ between the substrate materials (see Table). For Ge the normal-state resistance is much lower but the critical fields and currents are substantially smaller than in Si. The presented investigations show that the presence of superconducting Ga rich precipitates in heavily doped Ge should lead to an onset of superconductivity at critical temperatures comparable to amorphous Ga. The former studies of heavily Ga doped Ge show superconductivity only below 1 K.

Acknowledgments

Financial support by DFG (HE 2604/7-1) is gratefully acknowledged.

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