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Performance Comparison of QPSK Based Single and Double Stage Digital Interpolators

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In this paper, the performance of single stage and double stage digital interpolators has been compared and has been showed that by using multi stage interpolation system the reliability of any communication system increases drastically. Digital signal interpolation systems can be implemented in a variety of ways. The basic interpolator for up-sampling can be a combination of an expander unit with an interpolation low-pass filter in cascade. Complicated implementations can be done by connecting multiple expander and low-pass filter pairs in cascade. This paper presents the efficient implementation of digital interpolation systems for up-sampling of single stage and double stage digital interpolators by using quadrature phase shift keying technique. Comparison is done in terms of spectrum of generated signal, envelope power, modulated signal trajectory, input and output constellation and noise performance.

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1. Introduction

The process of digital signal interpolation is fundamental to signal processing. This paper explores efficient designs of digital interpolation systems for integer up-sample factors by using quadrature phase shift keying (QPSK) technique [1, 2]. The digital up-converter (DUC) provides interpolation, filtering, frequency translation, and summing of DUC channel outputs to produce digital IF outputs DUCs can be found in wireless base-station transmit electronics, specialized digital IF receive-test equipment, cable TV modulators, and software defined transmit-radio equipment. Test equipment and digital radio electronics typically use DUC devices combined with ADC and DAC to provide digital radio sections, or other specific applications such as receiver/transmitter test equipment [3, 4].

Fig. 1. Interpolation system consisting of an expander and low-pass filter.

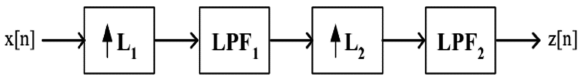

Fig. 2. Interpolation system consisting of the cascade of two expanders and two low-pass filters.

Interpolation of a signal by an integer up-sample factor can be accomplished by processing the signal, $x[n]$, with the cascade of an expander and low-pass filter, as shown in Fig. 1. If the input signal $x[n]$ has sampling frequency f, this results in the up-sampled and interpolated output signal $y[n]$ at the increased sampling frequency Lf. More complex interpolation systems can be designed as the cascade of multiple expanders and low-pass filters. A system containing two expanders and two low-pass filters is shown in Fig. 2 [5–7].

2. Materials and methods

For generating single stage and double stage interpolator, the QPSK technique has been used. Sometimes this is known as quaternary PSK, quadric-phase PSK, 4-PSK. With four phases, QPSK can encode two bits per symbol, shown in the diagram with gray coding to minimize the bit error rate (BER) — sometimes misperceived as twice the BER of BPSK. We have specifically used for simulation the pi/4 differential QPSK (DQPSK). All the results have been obtained using Agilent's Advanced Design System (ADS) software.

3. Experimental results and discussion

3.1. Single stage interpolator

The simulation diagram of the pi/4 DQPSK single stage interpolator may be shown in Fig. 3.

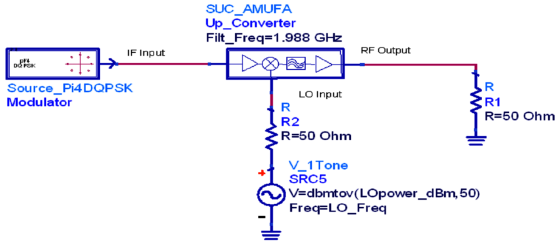

Fig. 3. Simulation diagram of the pi/4 DQPSK single stage interpolator.

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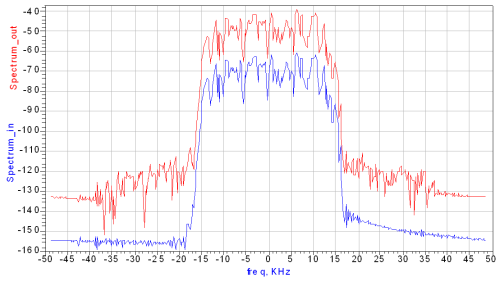

Fig. 4. Spectrum of generated signal for single stage interpolator.

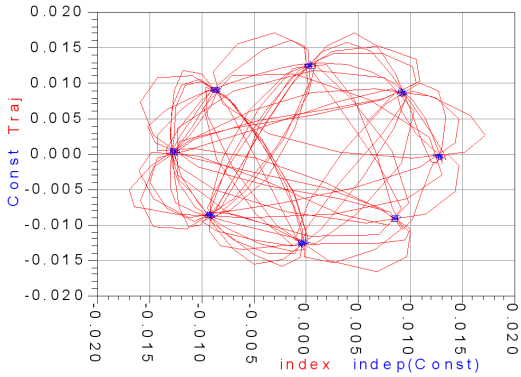

Fig. 5. Modulation signal trajectory and constellation.

The spectrum of generated signal for single stage interpolator may be shown in Fig. 4 and modulation signal trajectory and constellation may be shown in Fig. 5.

The total output power comes out to be −28.09 dB and peak to average is 3.181 dB and percentage error vector magnitude comes out to be 0.356 while noise performance calculated for amplifier-mixer USB-filter amplifier configuration is compiled in Table I.

TABLE I

Noise performance calculated for amplifier-mixer USB--filter amplifier configuration.

Parameter	Mix_{In} [dB m]	Mix_{Out} [dB m]	Filt_{Out} [dB m]	RF_{Out} [dB m]
power gain	−30.133	−36.838	−37.854	−27.815
cascade power gain	19.867	13.162	12.146	22.185
noise figure	4.001	7.080	7.082	7.133

3.2. Double stage interpolator

The simulation diagram of the pi/4 DQPSK double stage interpolator may be shown in Fig. 6.

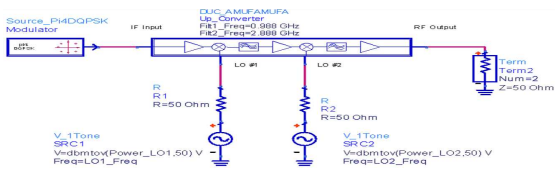

Fig. 6. Simulation diagram of the pi/4 DQPSK double stage interpolator.

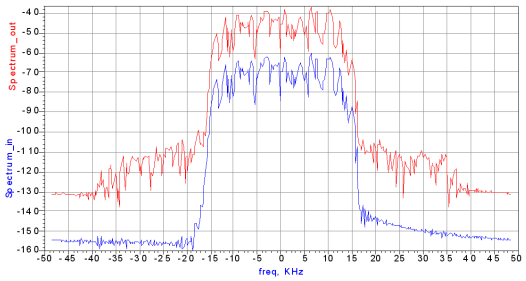

Fig. 7. Spectrum of generated signal for single stage interpolator.

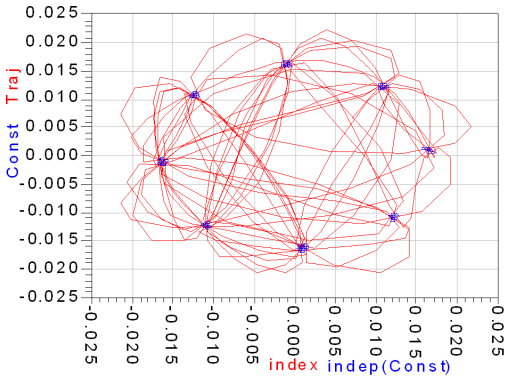

Fig. 8. Modulation signal trajectory and constellation.

The spectrum of generated signal for single stage interpolator may be shown in Fig. 7 and modulation signal trajectory and constellation are represented in Fig. 8.

The total output power comes out to be −25.84 dB m and peak to average is 3.158 dB and percentage error vector magnitude comes out to be 0.817 while noise performance calculated for amplifier-mixer USB--filter-amplifier-mixer USB-filter-amplifier configuration is compiled in Table II.

From the above results it is clear that double stage QPSK based interpolator is much better than single stage QPSK based interpolator.

4. Conclusion

The results in Tables I and II show that the use of QPSK based double stage interpolators results in increased power gain at different points of interpolator and cascade power gain also increases to an extent. Further to add, noise figure is now much better than the QPSK based single stage interpolators. Therefore, we can conclude that double stage interpolators are much more efficient and reliable than single stage interpolators.

TABLE II

Noise performance calculated for amplifier-mixer USB-filter-amplifier-mixer USB-filter-amplifier configuration.

Parameter	$Mix1_{In}$ [dB m]	$Mix1_{Out}$ [dB m]	$Filt1_{Out}$ [dB m]	$Mix1_{In}$ [dB m]	$Mix1_{Out}$ [dB m]	$Filt1_{Out}$ [dB m]	RF_{Out} [dB m]
power gain	−30.133	−36.856	−37.929	−27.869	−34.575	−35.591	−25.555
cascade power gain	19.867	13.144	12.071	22.131	15.425	14.409	24.445
noise figure	4.001	7.079	7.082	7.126	7.216	7.217	7.241

References

[1] A.Y. Kwentus, A.K.Z. Jiang, A.N. Willson Jr, *IEEE Trans. Signal Proc.* **45**, 457 (1997).

[2] C. Farrow, in: *Proc. IEEE Int. Symp. on Circuits and Systems (ISCAS88)*, 1998, p. 2642.

[3] D. Babic, M. Renfors, *IEEE Signal Proc. Lett.* **12**, 1 (2005).

[4] E.B. Hogenauer, *IEEE Trans. on Acoust. Speech Signal Proc. ASSP* **29**, 155 (1981).

[5] H. Oh, S. Kim, G. Choi, Y. Lee, *IEEE J. Select. Areas Commun.* **17**, 551 (1999).

[6] J. Vesma, Ph.D. Thesis, Tampere University of Technology, 1999.

[7] J. Vesma, T. Saramäki, *Filter Synthesis. Circ. Syst. Signal Proc.* **26**, 115 (2007).