

Reducing Leakage Power for SRAM Design Using Sleep Transistor

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Low power design is the industry buzzword these days in present chip design technologies. Caches occupy around 50% of the total chip area and consume considerable amount of power. This project's focus is to reduce leakage power consumption of an 8 kbit SRAM by employing techniques like power gating. The main technique used in power gating is the use of sleep transistor. In our design we have chosen a stack-based implementation.

DOI: 10.12693/APhysPolA.123.185

PACS: 85.40.–e

1. Introduction

CMOS technology scaling continues to reduce switching delay and power while improving area density [1]. As technology is scaled further, it brings challenging issues like process variations and increase in transistor leakage. A high performance VLSI microprocessor demands huge SRAM clusters to meet performance requirements. There are three components of the leakage power: sub-threshold leakage, gate leakage, and junction leakage. Lowering power supply or dropping the rail-to-rail voltage decreases the leakage power. By reducing the voltage, the SRAM cell stability is degraded but SRAM is required to retain the data. Hence, the rail-to-rail voltage needs to be carefully controlled to maintain cell stability, to avoid data loss [2].

As we can see from Figs. 1–4, the power leakage is getting worse with scaling [3]. Additionally since SRAM component of the design contributes much to the total chip area, their leakage power has become a significant component of total chip power.

2. Design and implementation

2.1. SRAM Cell — 6T

Using two cross coupled inverters, bit 0 or 1 is stored in a SRAM cell. This storage cell has two stable states 0 and 1 which is reinforced because of cross coupling. Two additional access transistors control the access to the storage cell during read and write operations. Access to the cell is enabled by the word line which controls the two access transistors M5 and M6. They in turn control whether the cell should be connected to the bit lines. Bit lines are used for both read and write operations. Two bit

lines are not necessary but they are provided to improve noise margins. So a typical SRAM cell is a six transistor structure. A 6T SRAM cell requires a careful device sizing to ensure read stability, write margin and data retention in standby modes. Figure 1 shows a typical 6T SRAM cell and Table I shows the corresponding transistor sizes. In read stability, M1 transistor is required to be much larger than M5 transistor to make sure that the node between M1 and M5 does not flip. In write mode, bit lines overpower cell with a new value. High bit lines must not overpower inverters during read operation. So, M2 is designed to be weaker than M5.

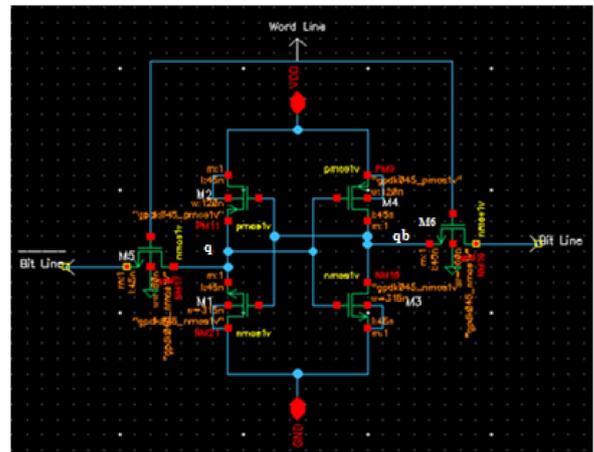


Fig. 1. SRAM cell.

2.2. Sleep transistors

Sleep transistors are generally high V_t . They are switched off when idle and can help save about 40% leakage power [4] as they help create virtual power and virtual ground networks. The virtual power network drives the

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TABLE I
Channel width and length
of each transistors.

Transistor	W/L [nm]
M1	315/45
M2	120/45
M3	315/45
M4	120/45
M5	160/45
M6	160/45

cells and can be turned off. The sleep transistors need to be tuned to a particular reference voltage by partially turning them on in idle mode.

As already mentioned in our design we have dynamically included sleep transistor in series with power supply to take advantage of the stack leakage savings. A critical design component — signal noise margin (SNM) will be significantly lowered by sleep transistors. To achieve a particular SNM, the size of the sleep transistor is to be scaled linearly with respect to the number of cells in a column. As with any design, there are tradeoffs associated with sleep transistors. Leakage current through sleep transistor is proportional to the width of the transistor. Small sleep transistors are more effective but they have negative impact on performance. When sleep transistors are upsized, leakage becomes less significant. Hence, sizing them is design dependent. In cases when delay could be tolerated, small sleep transistors are ideal for considerable power savings. In cases like adders which are delay critical, large sleep transistors are optimal.

2.3. Design of the sleep transistor

Size is calculated using the average current method [5]. When average current is flowing through the sleep transistor and speed penalty for the SRAM block is known,

the minimum size can be estimated [6]. Gate delay time of a CMOS circuit is $\tau(V_{dd}) = \alpha C V_{dd} / [\beta(V_{dd} - V_{tL})\alpha]$. Here β is drivability factor, C is output load capacitance, α is saturation index and V_{tL} is low V_{th} . MTC-MOS speed penalty is $MSP = 1/[1 - (I_{sleep}/W_{sleep}) - (R'/(V_{dd} - V_{tL}))\alpha - 1]$ where R' is normalized sleep transistor resistance width of sleep transistor $W_{sleep} = \{1/[1 - MSP(1/1 - \alpha)]\}[R'/(V_{dd} - V_{tL})]I_{sleep}$ [7].

The voltage swing is given by $\Delta V = I_{sleep}R_{sleep}$. If W_{sleep} is too large the current resonators suppress large ground forces and will not switch if it is too small the ground bounce is up to $0.5V_{dd}$. So typically the sleep transistor is 3% of SRAM cell area. In Fig. 2 there is our SRAM cell with the sized sleep transistors [8].

2.4. Sleepy SRAM cell — 10T

Two pairs of sleep transistors are used in the SRAM cell as shown in Fig. 2. One in each pair is activated during idle mode based upon the value of the bit stored in the cell. This disconnects the OFF transistors from supply while retaining supply to the ON transistors [9]. Table II shows the corresponding transistor sizes.

TABLE II
Channel width and length
of each 10T transistor.

Transistor	W/L [nm]
N1	315/45
N2	315/45
N3	315/45
N4	315/45
N5	160/45
P1	120/45
P2	120/45
P3	120/45
P4	120/45
N6	160/45

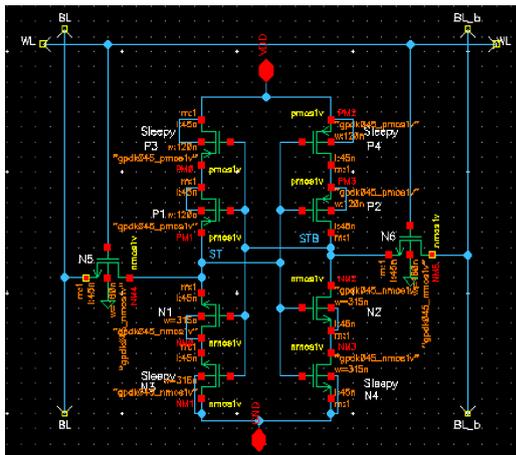


Fig. 2. 10T SRAM cell.

3. Results

In this paper, leakage power is measured by simulating a 1 Kb SRAM array. Leakage power is measured when each SRAM cell holds a logical “1” or “0”. Simulations were done in CADENCE using 45 nm technology. The leakage power of 10 T SRAM cell (Sleepy) and 6T SRAM cell is shown on Figs, 3 and 4.

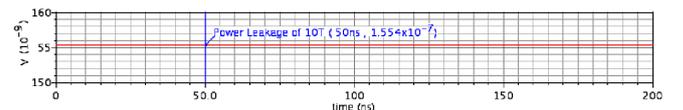


Fig. 3. Leakage power of 10T SRAM cell (sleepy) = 155.4 nW.



Fig. 4. Leakage power of 6T SRAM cell (non-sleepy) = 375.3 nW.

TABLE III
Leakage power in various sleepy modes.

Mode	Leakage power [mW]	Reduction rate
100% sleepy	19.36	47%
75% sleepy	23.28	37%
50% sleepy	27.58	25%
25% sleepy	31.90	13%
non sleepy	36.52	0

Table III shows the leakage power and rate of reduction associated with the different kinds of implementation. Since, this is only for 1 Kb design, the reduction rate increases further as we move to higher density SRAM designs.

Acknowledgments

This work was supported by ITM University Gwalior, with collaboration Cadence Design System Bangalore. The authors would also like to thank to Professor R.D. Gupta for his enlightening technical advice.

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