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Electrical Properties of *p*-ZnTe/*n*-CdTe Photodiodes

S. Chusnutdinow[a], V.P. Makhniy[b], T. Wojtowicz[a] and G. Karczewski[a]

[a]Institute of Physics, Polish Academy of Sciences, al. Lotników 32/46, 02-668 Warsaw, Poland
[b]Yuri Fedkovych Chernivtsi National University, 2 Kotsyubynsky Str., 58012 Chernivtsi, Ukraine

Current–voltage (I–V) and capacitance–voltage (C–V) characteristics of photovoltaic, thinfilm p-ZnTe/n-CdTe heterojunctions have been studied in the temperature range of 280–400 K. The p–n junctions were grown by MBE on (100) semi-insulating GaAs substrates. From the analysis of I–V and C–V curves the potential barrier height of the junctions and its temperature dependence are determined. The relatively large value of the temperature coefficient of the potential barrier height (2.5–3.0×10^{-3} eV/K) indicates a high density of defects at the p-ZnTe/n-CdTe interface. The presence of interface defects limits the efficiency of the solar energy conversion of these devices.

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1. Introduction

Heterojunctions with photosensitive layers of CdTe belong to the most promising devices for converting solar energy into electricity [1]. Among them n-CdS/p-CdTe solar cells exhibit the record energy conversion efficiency of 16.5% [2]. This record, however, is still far from the theoretical limit of 28% [1]. In order to enhance the energy conversion efficiency further optimization of technology is required. In particular, a reduction of electrical contact resistivity of the solar cells would certainly improve their parameters. Low-resistivity contacts to p-CdTe layers are difficult to manufacture. The problem can be solved by depositing p-type ZnTe layer with high carrier concentration of 10^{18}–10^{19} cm^{-3} [3, 4].

On the other hand, p-ZnTe forms heterojunction with n-type CdTe. In this case ohmic contacts to both sides on the junction are not difficult to achieve. In addition, the theoretical limit for the solar energy conversion efficiency is relatively high — it exceeds 20%. Because of these reasons the p-ZnTe/n-CdTe heterojunctions are interesting candidates for solar applications [5, 6].

In this work we analyze electric properties of light-sensitive, thin-film p-ZnTe/n-CdTe heterostuctures grown by molecular beam epitaxy (MBE).

2. Experimental

The investigated p-ZnTe/n-CdTe hetrostructures were grown by MBE on semi-insulating, (100)-oriented GaAs substrates in ultrahigh vacuum EPI 620 MBE system. Firstly, a 13 μm thick, highly iodine doped n-type CdTe buffer was grown on a (100) oriented GaAs substrate. In order to increase the electron concentration in the buffer the growth temperature was reduced to about 250 °C. The best contact layers grown in this way exhibit the electron concentration of 8–9×10^{18} cm^{-3} and resistivity of 1–2×10^{-2} Ω cm. These parameters are comparable to the best n-type doped ZnO contact layers. The n-CdTe buffer was covered by 2 μm thick, undoped CdTe and subsequently by 0.2 μm of nitrogen-plasma doped p-type ZnTe. For the growth of the intrinsic CdTe and p-type ZnTe the growth temperature was elevated to 300 °C. An ohmic contact to the p-side was formed by chemical deposition of gold.

Prior to formation of the ohmic contact to the n-type CdTe layer the top-most layers of intrinsic CdTe and p-type ZnTe were removed by etching in Br-methanol and the contact was formed by In soldering to the n-type CdTe buffer, as shown in the inset to Fig. 1. The resulting p–n junctions exhibit strong rectifying properties with the rectifying coefficient exceeding 10^5 at $T = 300$ °C and voltage of 1 V, as shown in Fig. 1.

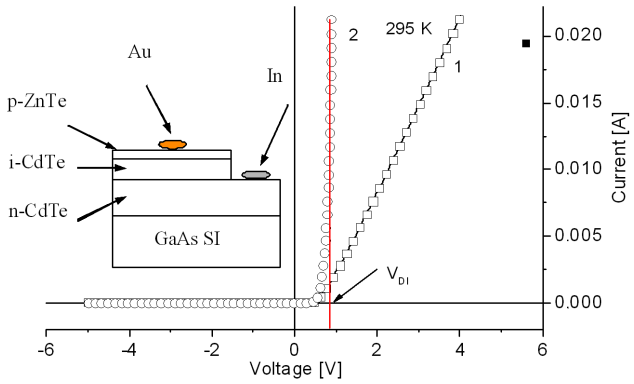

Fig. 1. I–V characteristics of a n-CdTe/p-ZnTe heterojunctions. The inset shows the investigated structure. Solid lines — extrapolation of experimental results.

For measurements of current–voltage (I–V) characteristics a source-meter Keithley 2601 has been used. The capacitance–voltage (C–V) characteristics were measured by Hewlett-Packard HP 4275 capacitance-meter at the frequency of 10 kHz and the signal amplitude of 30 mV.

Since the investigated p-ZnTe/n-CdTe heterostructures are intended to work as solar energy converters, the measurements were carried out in the vicinity of the room temperature, from 280 up to 400 K. The upper temperature was limited by the melting temperature of indium.

3. Results and discussion

Figure 1 shows a typical current–voltage (I–V) characteristic of a p-ZnTe/n-CdTe diode in linear coordinates. The high-voltage, linear part of the I–V curve is strongly influenced by a series resistance of the diode. The diode series resistance can be estimated from the differential resistance of the diode voltage versus bias voltage $R_{\rm dif}(V)$ as shown in Fig. 2. With increasing bias voltage $R_{\rm dif}$ sharply decreases and at about 2.0 V saturates at the value of 145 Ω, i.e., at the value of the series resistance. The I–V curve corrected by subtraction of the series resistance is shown in Fig. 1 by curve 2.

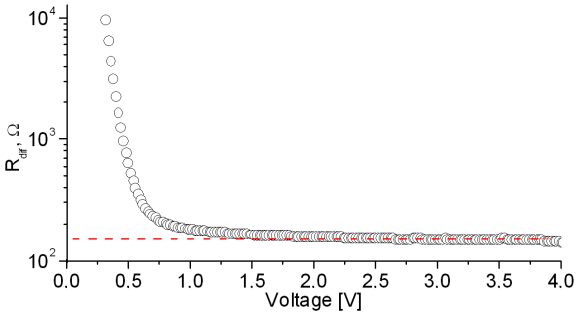

Fig. 2. The differential resistance of the diode at 295 K.

The diffusion voltage, determined from I–V curve as shown in Fig. 1, is a measure of the junction potential barrier height, $eV_{\rm DI}$. As shown in Fig. 3, $V_{\rm DI}$ linealy decreases with the increasing temperature. The experimentally determined temperature coefficient of $V_{\rm DI}$, $\beta_{\rm I} = 2.5 \times 10^{-3}$ V/K, appears to be almost one order of magnitude larger than the temperature coefficient of the energy gap, which for CdTe equals to 4.9×10^{-4} eV/K [7]. The high value of $\beta_{\rm I}$ indicates a high density of surface defects, $N_{\rm s}$, at the CdTe/ZnTe interface. The defects are generated by the large lattice mismatch in this material system. In the first approximation, the defects density at the interface is a function of a distance between surface dislocations, x: $N_{\rm S} \sim x^{-2}$, where

$$x = \frac{a_1 a_2}{|a_1 - a_2|}. \qquad (1)$$

Taking into account $a_1 = 6.46$ Å and $a_2 = 6.088$ Å for CdTe and ZnTe, respectively, the surface defect density $N_{\rm S} = 3 \times 10^{13}$ cm^{-2}. Not all of the defects are expected to be electrically active, however, their high density influences the potential barrier height of the junction and thus determines carrier transport mechanisms across the junction.

It has to be noticed that the diffusion voltage extrapolated to 0 K gives the value of the potential barrier of $eV_{\rm DI} = 1.5$ eV which is very close to the energy gap of CdTe. This means that the space charge region of the junction is located in the intrinsic CdTe layer. The I–V data do not provide, however, any information about the shape of the junction potential barrier.

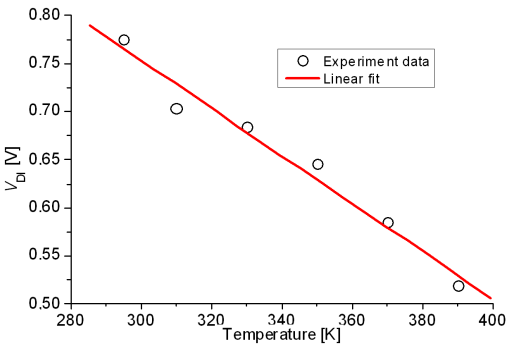

Fig. 3. Dependence of the $V_{\rm DI}$ on the temperature.

Information about the potential shape can be obtained from capacitance–voltage measurements. The junction capacitance can be described by the C^{-2}–V scale, it is shown in Fig. 4. A linear extrapolation of the $C^{-2}(V)$ function to $V = 0$ provides an alternative method of determination of the diffusion voltage, $V_{\rm DC}$. The diffusion voltage determined from capacitance measurements appears to be slightly higher than the same parameter determined from current measurements — for instance, at $T = 300$°C $V_{\rm DC} = 1.16$ V and $V_{\rm DI} = 0.76$ V. This discrepancy of these results with the I–V based results can be explained by the frequency dependence of the capacitance measurements.

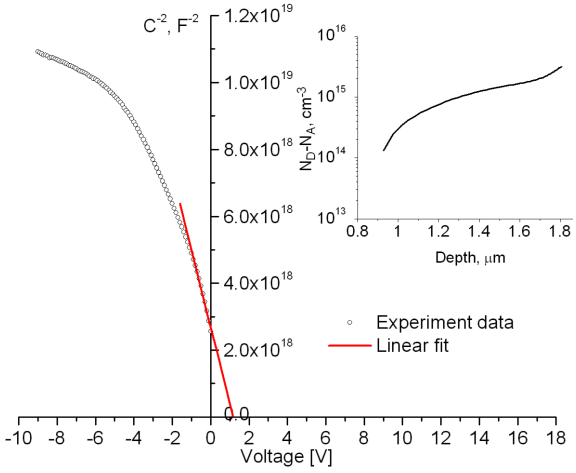

Fig. 4. C–V characteristics of a n-CdTe/p-ZnTe heterojunctions. The inset shows depth profiles of the net donor concentration in the intrinsic CdTe layer. Solid lines — extrapolation of experimental results.

The capacitance diffusion voltage, $V_{\rm DC}$, is proportional to the inverse temperature. The temperature coefficient of this dependence, $\beta_{\rm C} = 6.7 \times 10^{-3}$ V/K, is close to $\beta_{\rm I}$, which confirms the high concentration of the defect states at the CdTe/ZnTe interface.

Figure 4 shows that the $C^{-2}(V)$ curve is not linear in entire range of the bias voltage which indicates that the charge density is not uniform over the space charge re-

gion. The depth profiles of the net donor concentration can be calculated by using the following expression:

$$N_{\mathrm{D}} - N_{\mathrm{A}} = \frac{2}{q\varepsilon_{\mathrm{S}}\varepsilon_0 A^2}\left[\frac{1}{\mathrm{d}(1/C^2)/\mathrm{d}V}\right], \tag{2}$$

$$W = \frac{\varepsilon_{\mathrm{S}}\varepsilon_0 A^2}{C}, \tag{3}$$

where C denotes the depletion capacitance, W — the depletion layer width, $N_{\mathrm{D}} - N_{\mathrm{A}}$ — the net donor concentration, A — the effective area of the diode was 0.06 cm^2, q — the elementary charge, ε_0 — the dielectric constant in vacuum, ε_{S} — the relative dielectric constant, and V — the DC bias voltage [8]. The relative dielectric constant of CdTe, $\varepsilon_{\mathrm{S}} = 10.4$ was used [7]. The width of the space charge region, W, is determined from Eq. (3) and is equal to 0.9 μm at $V = 0$. The obtained result shows that the space charge region is half as thick as the intrinsic CdTe layer. The depth profile of the net donor concentration is shown in the inset to Fig. 4.

The interface defects influence the current flow across the p–n barrier. As shown in Fig. 5 the current across the p-ZnTe/n-CdTe heterojunctions can be described by the diode Shockley equation

$$I = I_0 \exp(q(V - IR_{\mathrm{s}})/nkT), \tag{4}$$

where I_0 is the reverse saturation current and n — the diode ideality parameter. The ideality parameter decreases from 1.5 at 290 K to 1.0 at 390 K, which indicates that with the increasing temperature the current flow mechanisms change. In the vicinity of the room temperature ($n = 1.5$) the diode current is limited by recombination of carriers in the space charge region. The recombination processes play an important role when the potential barrier is relatively high — higher than half of the energy gap. Such a situation takes place in our case at the room temperature $eV_{\mathrm{CD}} = 1.0$ V $> (1/2)E_{\mathrm{g}} = 0.8$ V. With the increasing temperature the barrier height decreases, the above inequality changes its direction and the recombination in the space charge region becomes less important. The carrier emission over the potential barrier becomes dominant for the diode current. For this current mechanism the ideality factor should be equal to 1, which is indeed observed in the experiment.

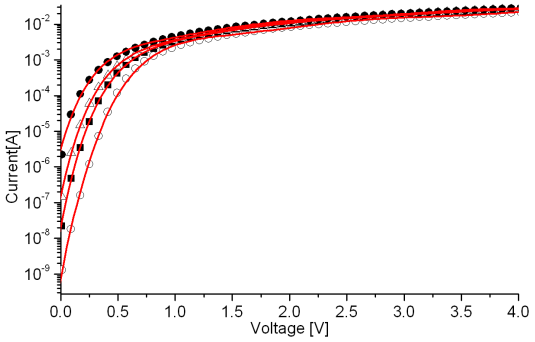

Fig. 5. The forward bias current–voltage characteristic curves at different temperatures. Solid curves are theoretic and described by Eq. (4).

At higher forward bias the diode current inclines from the exponential dependence as shown in Fig. 5. This is caused by the series resistance of the heterojunction. At $T = 300$ K the series resistance is relatively high, $R = 145\ \Omega$, which limits the external quantum efficiency of the devices as solar energy convertors to the value of 3–4%.

4. Conclusions

Thin-film p-ZnTe/n-CdTe heterojunctions grown by MBE were characterized by C–V and I–V measurements. From the analysis of experimental data curves the potential barrier height and its temperature dependence were determined. The relatively large value of the temperature coefficient of the potential barrier voltage ($\approx 2.5 \times 10^{-3}$ eV/K) indicates that the concentration of defects at the p-ZnTe/n-CdTe interface is as high as 3×10^{13} cm^{-3}. The high defect density together with the high series resistance of the junction limit the solar conversion efficiency to 3–4%. We propose that in order to improve performance of the CdTe–ZnTe solar cell one could use graded CdZnTe layer. This would reduce the number of a lattice mismatch related defects.

Acknowledgments

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