41th "Jaszowiec" International School and Conference on the Physics of Semiconductors, Krynica-Zdrój 2012

Electrostatic Gates for GaN/AlGaN Quantum Point Contacts

M. CZAPKIEWICZ^a, G. CYWIŃSKI^b, K. DYBKO^a, M. SIEKACZ^b, P. WOLNY^b,

S. GIERAŁTOWSKA^a, E. GUZIEWICZ^a, C. SKIERBISZEWSKI^b AND J. WRÓBEL^a

^aInstitute of Physics, Polish Academy of Sciences, al. Lotników 32/46, 02-668 Warszawa, Poland

^bInstitute of High Pressure Physics, Polish Academy of Sciences, Warsaw, Poland

We report on AlGaN/GaN quantum point contacts fabricated by using e-beam lithography and dry ion etching. The tunable nano-constrictions are defined by the integration of side and top gates in a single device. In this configuration, the planar gates are located on the both sides of a quantum channel and the metallic top gates, which cover the active region, are separated from the substrate by an insulating and passivating layers of HfO₂ or Al₂O₃/HfO₂ composite. The properties of devices have been tested at T = 4.2 K. For side gates we have obtained a very small surface leakage current $I_{\rm g} < 10^{-11}$ A at gate voltages $|V_{\rm g}| < 2$ V, however, it is not enough to close the quantum channel. With top gates we have been able to reach the pinch-off voltage at $V_{\rm g} = -3.5$ V at a cost of $I_{\rm g} \approx 10^{-6}$ A, which has been identified as a bulk leakage current.

PACS: 73.40.Qv, 73.61.Ng, 73.23.-b

1. Introduction

High electron mobility transistors (HEMT) based on the GaN/AlGaN heterostructure are very promising candidates as chemical and biological sensors since its sheet carrier density is strongly influenced by the surface potential [1]. Furthermore, an opportunity of integration with solar blind UV detectors or high temperature, high power electronics makes GaN-based HEMT structures to be used for a variety of applications [2]. However, a strong dependence of carrier concentration on the ambient conditions creates also a major obstacle for fabrication of ballistic nanostructures, like quantum point contacts (QPCs) or quantum dots (QD), from this material. For example, QDs produced in GaN by so-called *split-gate* technique are very sensitive to the presence of randomly charged surface states and often their proper action suffers from a large gate current leakage [3]. Therefore, the challenge for a construction of such devices is to optimize the technology and performance of the electrostatic Schottky gates towards reduction of parallel (surface and substrate) conduction and trapping effects. For that, the passivation with dielectric layer is often applied in order to reduce the surface states on GaN or AlGaN [4].

In this work we describe the fabrication of tunable nano-constriction by means of *etching* narrow grooves which define the contact itself, but also the planar gates located on the both sides of a quantum channel. Additionally, a metallic (Au) top gate is applied which covers the active region of the device and is separated from the substrate by an insulating and passivating layers of the hafnium oxide HfO₂ or Al₂O₃/HfO₂. Side gates are known to produce excellent and adiabatically smooth constrictions on GaAs/AlGaAs heterostructures [5, 6] and the metal gate over the active region of the device helps to symmetrize transmission coefficients by screening surface states and smoothing the confinement potential [7]. We believe that the combination of side/ top gates, which is for the first time applied for GaN/Al-GaN nanostructurization, can provide an additional control over one-dimensional (1D) carrier density and leakage currents in this material.

2. Materials and results

For our studies we used two distinct high mobility GaN/AlGaN structures, which have been grown by plasma assisted molecular beam epitaxy (PAMBE). The sequence of epitaxial layers for both substrates is shown in Fig. 1a. For sample A, the two-dimensional electron gas (2DEG) is located very shallow under the surface (13 nm), whereas for sample B corresponding distance is larger (29 nm). This makes sample A more fragile to the gate-2DEG leakage, however, the additional laver (500 nm GaN:Mg) has been introduced to reduce the buffer leakage as compared to sample B. From the Hall effect measurements the low-temperature (T = 4.2 K) mobilities $\mu_{\rm e} = 2.2 \times 10^5 \text{ cm}^2/(\text{V s})$ and $4.5 \times 10^5 \text{ cm}^2/(\text{V s})$ have been obtained for samples A and B, respectively, with 2D electron densities $n = 3.1 \times 10^{12} \text{ cm}^{-2}$ (A) and $2.4 \times 10^{12} \text{ cm}^{-2}$ (B) (in dark).

Four-terminal quantum point contacts with lithographic width $W_{\text{lith}} = 0.4, 0.6, \text{ and } 0.8 \ \mu\text{m}$ have been patterned by e-beam lithography and inductively coupled plasma reactive ion etching (ICP RIE) with PMMA resist used as an etching mask. For that, the optimization of etching parameters was needed since PMMA is very sensitive to plasma processing. The best results have been obtained for etching rates \approx 60 $\rm nm/50~s$ for GaN and $\approx 360 \text{ nm}/50 \text{ s}$ for PMMA. With these parameters the V-shaped side-gates, separated from the constriction area by ≈ 60 nm deep etched grooves, have been successfully defined on top of macroscopic Hall-bar structures (see Fig. 1b). Let us note the smooth edges of separating grooves with roughness which favourably compares to the results of a wet chemical etching [5, 6]. Unfortunately, the dry plasma processes create depletion regions



Fig. 1. (a) Two GaN/AlGaN heterostructures grown by PAMBE technique. The sequences of epitaxial layers are shown for samples A and B (schematically). (b) Scanning electron microscope (SEM) micrograph of quantum point contact formed by dry etching. Separating grooves are marked with arrow, depth of etching 60 nm.



Fig. 2. (a) SEM micrograph of quantum point contact already covered by top-gate layers (side view). (b) Magnified image of the gate edge deposited on sample A, dielectric (HfO₂) and metal (Au) layers are clearly visible, the widths of films are indicated in (c). (d) Cross-section of gate films (HfO₂/Al₂O₃/Au) deposited on sample B.

on the mesa walls, it may explain why the measured conductance G of our devices is not monotonic as a function of W_{lith} .

On GaN substrates the dielectric SiN layers grown by plasma deposition are typically applied for the surface passivation [8, 9]. Recently, however, better results have been obtained for atomic layer deposited (ALD) HfO₂ [10] and Al₂O₃ [4] films, which are characterized by high dielectric constant and high breakdown field. Furthermore, the ALD technique is well fitted to electron beam lithography methods, since the low deposition temperature permits a film growth without the hard-baking of resist and lift-off processes give smooth edges with roughness as low as 10 nm [11].

Therefore, in this work we used 30 nm HfO₂ (on sample A) and 100 nm composite HfO₂/Al₂O₃ (on sample B) as insulator layers, both produced by low growth temperature ($T_{\rm g} \leq 100$ °C) atomic layer deposition process [12]. Dielectric films were patterned by e-beam lithography and *lift-off* technique. Prior to lift-off, oxide layers have been covered with 30 nm Au metal gate, results are shown in Fig. 2.

To characterize electrically the patterned devices the I-V characteristics have been obtained at temperature

T = 4.2 K before the deposition of top gates. Side gate current $I_{\rm g}$ has been measured as a function of gate voltage $V_{\rm g}$ applied between both gates and one of the ohmic contacts. At the same time the differential conductance G of the constriction vs. $V_{\rm g}$ has been also recorded using the low-frequency lock-in technique. The same procedure has been repeated for the top gates after the deposition of insulator and metal films. Top gates have been contacted with the conducting epoxy, since the bonding machine cannot be applied on a fragile amorphous substrates. Results for samples A and B are summarized in Figs. 3 and 4, respectively.



Fig. 3. Gate current I_g and differential conductance G (in $G_0 = 2e^2/h$ units) as a function of gate voltage V_g for sample A. (a) Gate current (solid lines, left logarithmic scale) and conductance (dotted lines, right scale) as a function of side-gate voltage (before top-gate deposition) for several devices with $W_{\rm lith}$ indicated in legend. (b) Gate current vs. top-gate voltage for devices with $W_{\rm lith} = 600$ nm and 800 nm.



Fig. 4. Gate current $I_{\rm g}$ and differential conductance G (in $G_0 = 2e^2/h$ units) as a function of gate voltage $V_{\rm g}$ for sample B and QPC with $W_{\rm lith} = 600$ nm. (a) Gate current (red line, right logarithmic scale) and conductance (blue line, left scale) as a function of side-gate voltage (before top-gate deposition). (b) Gate current (red line, right logarithmic scale) and conductance (blue line, left scale) as conductance (blue line, right logarithmic scale) and conductance (blue line, right logarithmic scale) and conductance (blue line, left scale) vs. top-gate voltage.

For sample A (with shallow 2DEG) we have observed practically no current leakage ($I_{\rm g} < 2 \times 10^{-11}$ A) in the voltage range -2 to +2 V for planar gates (Fig. 3). This is a promising result, which shows that the etched grooves separate effectively gate areas from other parts of the sample and no surface leakage is detected. Unfortunately, such voltage range is too small for an efficient control of the channel conductance. Furthermore, covering the sample A with the top gate has not solved the problem. After the process a large top gate current $I_{\rm g} \approx 10^{-6}$ A was measured, already at $V_{\rm g} = 0.4$ V. Very probably, the

applied insulator layer (HfO_2) is too thin (30 nm) for samples with shallow 2DEG, like sample A.

For side-gates on sample B (with deeper 2DEG) we have obtained a much larger gate leakage $I_{\rm g} \approx 10^{-6}$ A for side-gate voltage $|V_{\rm g}| < 2$ V (Fig. 4a). This is probably related to the buffer leakage current which is reduced in sample A. Apart from this, the transconductance has been very small and again insufficient to close the quantum channel in the range -2 to +2 V, quite similarly to sample A. Interestingly, for $|V_{\rm g}| > 1.7$ V a dramatic increase of QPC current noise is observed, which also corresponds to the increase of $I_{\rm g}$, marked with arrows in Fig. 4a. Most probably, the appearance of noise highlights the onset of direct gate-channel tunnelling and again limits the effective range of side-gate operation to $|V_{\rm g}| < 2$ V voltage range.

Fortunately, for sample B we have been able to completely close the quantum channel at pinch-off voltage of -3.5 V and also to increase the conductance up to $13G_0$ for $V_{\rm g} = +3$ V (Fig. 4b). This result shows that the topgate alone can be used to control the channel, however, at a cost of considerable gate leakage ($I_{\rm g} \approx 2 \times 10^{-7}$ A at $V_{\rm g} = -2$ V). On the other hand, no noise increase is observed, which suggests that the source of leakage for sample B is a buffer current. Finally, no hysteresis in upand down-gate voltage sweeps has been observed, which indicates that the oxide layer effectively passivates surface states.

3. Summary and conclusions

In summary, we have demonstrated the QPCs fabricated from GaN/AlGaN heterostructures by using e-beam lithography and dry ion etching. The tunable nano-constrictions have been defined by the integration of sidegates, insulator layers and top gates in a single device. In this configuration, the planar gates are located on the both sides of a quantum channel from which they are separated by deep etched trenches. The active region of the QPC is covered with insulating and passivating layers of HfO₂ or Al₂O₃/HfO₂ composite and capped with metal (Au) top-gate film.

We have studied the differential conductance of QPCs and I-V characteristics of both types of electrostatic gates at liquid helium temperatures. For side gates we have observed very small surface leakage current $I_{\rm g} < 10^{-11}$ A, however, the obtained transconductance is very small and the effective range of operation is limited to voltages $|V_{\rm g}| < 2$ V.

For top gates the measured transconductance is much larger, it was sufficient to close the quantum channel of $W_{\rm lith} = 600$ nm already at $V_{\rm g} = -3.5$ V, for sample covered with 100 nm HfO₂/Al₂O₃ composite. Furthermore, the top-gate with 30 nm HfO₂/30 nm Au layer sequence turn out to be unacceptably leaky on sample with shallow 2D electron gas.

In conclusion, the side gate/top gate combination, which served well for GaAs/AlGaAs system, can be ap-

plied also to the design of electrostatic gates on GaN/ AlGaN heterostructures. Combined with surface passivation, provided by unique properties of Al_2O_3/HfO_2 dielectrics, such design may provide a stability and reproducibility which are key ingredients of quantum transport studies. To achieve this goal at least two elements have to be improved. First, the buffer leakage must be strongly reduced by a proper design of epitaxial and probably also top metal layers. Second, to maximize the side gates performance, the width of separating grooves and the size of depletion region should be reduced.

Acknowledgments

We acknowledge the support from the Polish Ministry of Science and Higher Education, project number N202/ 103936 and by the European Union within European Social and Regional Development Founds, through grant Innovate Economy (POIG.01.01.02-00-008/08).

References

- M. Stutzmann, G. Steinhoff, M. Eickhoff, O. Ambacher, C. Nebel, J. Schalwig, R. Neuberger, G. Müler, *Diamond Relat. Mater.* 11, 886 (2002).
- [2] Nitride Semiconductor Devices: Principles and Simulation, Ed. J. Piprek, Wiley, Weinheim 2007.
- [3] H.T. Chou, D. Goldhaber-Gordon, S. Schmult, M.J. Manfra, A.M. Sergent, R.J. Molnar, Appl. Phys. Lett. 89, 033104 (2006).
- [4] Z.H. Liu, G.I. Ng, H. Zhou, S. Arulkumaran, Y.K.T. Maung, Appl. Phys. Lett. 98, 113506 (2011).
- [5] A. Kristensen, H. Bruus, A.E. Hansen, J.B. Jensen, P.E. Lindelof, C.J. Marckmann, J. Nygärd, C.B. Sörensen, F. Beuscher, A. Forchel, M. Michel, *Phys. Rev. B* 62, 10950 (2000).
- [6] M. Czapkiewicz, P. Zagrajek, J. Wróbel, G. Grabecki, K. Fronc, T. Dietl, Y. Ohno, S. Matsuzaka, H. Ohno, *Europhys. Lett.* 82, 27003 (2008).
- J. Liu, W.X. Gao, K. Ismail, K.Y. Lee, J.M. Hong, S. Washburn, *Phys. Rev. B* 50, (1994).
- [8] N.-Q. Zhang, S. Keller, G. Parish, S. Heikman, S.P. DenBaars, U.K. Mishra, *Electron Dev. Lett. IEEE* 21, 421 (2000).
- [9] Y.F. Wu, A. Saxler, M. Moore, R.P. Smith, S. Sheppard, P.M. Chavarkar, T. Wisleder, U.K. Mishra, P. Parikh, *Electron Dev. Lett. IEEE* 25, 117 (2004).
- [10] A. Koudymov, N. Pala, V. Tokranov, S. Oktyabrsky, M. Gaevski, R. Jain, J. Yang, X. Hu, M. Shur, R. Gaska, G. Simin, *Electron Dev. Lett. IEEE* **30**, 478 (2009).
- [11] M.J. Biercuk, D.J. Monsma, C.M. Marcus, J.S. Becker, R.G. Gordon, *Appl. Phys. Lett.* 83, 2405 (2003).
- [12] S. Gierałtowska, D. Sztenkiel, E. Guziewicz, M. Godlewski, G. Łuka, B. Witkowski, T. Wachnicki, E. Łusakowska, T. Dietl, M. Sawicki, Acta Phys. Pol. A 119, 333 (2011).