# Electrical Behaviour of Nanostructured Porous Silicon

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The electrical behaviour of porous silicon layers has been investigated on one side of p-type silicon with various anodization currents, electrolytes, and times. Electron microscopy reveals the evolution of porous silicon layer morphology with variation in anodization time. In this work electrical conductivity of bulk silicon and porous layer which is formed by electrochemical etching is compared due to I-V measurements and calculation of activation energy. We have also studied the dependence of porous silicon conductivity on fabrication conditions. Also the effect of the temperature on conduction of porous silicon at different frequencies is investigated. At last dependence of capacitance on the temperature was probed at  $10^2-10^5$  Hz frequency range.

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## 1. Introduction

Porous silicon (PS) is a material that has been made by etching process with electrochemical anodization method on bulk silicon surface. The material showed different properties compared with silicon. In the recent decades much investigation has been paid to the physical properties of PS [1]. The attractive optoelectronic properties of porous silicon along with the low cost fabrication posibilities have paved new ways for the development of this photoluminescent material [2–4]. Progress in PS optoelectronics depends on understanding of the operating principles of PS device structures [5]. While the optical properties of PS have been extensively studied, the electrical properties and conduction mechanisms, though of prime import, still have some contentious issues associated with them [6–11].

Owing to its large specific surface area and arts, porous silicon as a promising gas or humidity sensing material has attracted much attention in the past several years [12, 13]. A nanoporous pillar array (Si-NPA) might be a promising sensing material to fabricate practical room--temperature ethanol gas sensors [14]. This material has recently been discussed as a novel transducer material for chemical sensors and biosensors [15–17]. This is due to the fact that the preparation of PS by means of an anodic etching process is fully compatible to the semiconductor processing in sensor fabrication [18].

#### 2. Experimental

The porous layers are prepared by electrochemical anodization of *p*-type, monocrystalline polished silicon wafers of (100) orientation with 2–5  $\Omega$  cm resistivity range. An ohmic contact was obtained through thermal evaporation of a thin aluminium film with the thickness of 30–40 nm, to the backside of the wafer. During anodization, this backside was covered with an acid-proof

wax for protection. The PS layers were obtained by electrochemical etching in a  $HF(40\%)/ethanol(99.8\%)/H_2O$ solution. The electrochemical etching was carried out at various current densities, anodization time and HF concentration, and then air-dried. After anodization a thin Au film with 20–30 nm thickness was coated on the PS layers to create a semitransparent ohmic electrical contact without filling the pores. We checked by scanning electron microscopy (SEM) pictures that the evaporated Au did not fill the pores, and also the morphology of PS samples was observed with SEM. The measurements were carried out by putting the device in a chamber. Current was measured using a Keithley 610C electrometer. The measured current was in the range of milliamperes. An inductance-capacitance-resistance (LCR) multi-frequency meter was used to probe the variation of the capacitance of PS layer with temperature. All these measurements were carried out under atmospheric pressure and held in dark.

### 3. Results and discussion

PS preparation with different anodization parameters are given in Table.

According to the diameter of pores as shown in Fig. 1, the porous layers fabricated under above conditions are mesoporous. Mesoporous form (crystallites size around 10–100 nm) allows thick and mechanically stable porous layer production. It is known as an electrical semi-insulator even at low porosity [19].

The characteristic current–voltage (I-V) curves correspond to a PS sample  $(S_2)$  and bulk silicon shows that conductivity of PS sample is reduced (Fig. 2). It is due to an increase in the resistance of porous silicon. We can explain this by an increase in the band gap of PS. To investigate this we measured current at different temperatures and fixed voltage 0.5 V. Activation energy of bulk silicon and PS was calculated due to curve slope, Figs. 3 and 4, respectively, 0.315 eV and 0.515 eV. These figures show that after porosity activation energy increased, so the band gap is increased.

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Characteristic of porous silicon with various parameters.

Sample	Anodization time [min]	${f Current}\ {f density}\ [mA/cm^2]$	Electrolyte ratio (HF:ethanol:H <sub>2</sub> O)	$_{\rm pH}$	$egin{array}{c} { m Sample} \\ { m area} \\ [{ m cm}^2] \end{array}$	Porosity [%]
$S_1$	25	20	2:2:1	2.1	1	50
$S_2$	25	20	1:2:2	2.5	1	36
$S_3$	25	30	1:2:2	2.5	1	45
$S_4$	30	20	1:2:2	2.5	1	40
$S_5$	40	20	1:2:2	2.5	1	31



Fig. 1. Top view scanning electron micrographs of PS sample fabricated with different anodization time: (a) 25 min  $(S_2)$  at 30000 magnification, (b) 30 min  $(S_4)$  at 30000 magnification, (c)  $S_2$  at 60000 magnification, diameter of pore is 17 nm, (d)  $S_4$  at 60000 magnification, diameter of pore is 19 nm.

We also measured electronic current-voltage characteristics for a Au/PS/Si/Al sandwich structure. Figure 5 shows that conductivity of PS depends on anodization parameters, decreasing with pH of electrolyte and current density, because the porosity increases. Porosity and consequently conductivity depend on anodization time, porosity increases with anodization time and reaches roughly the saturation [20], which seems to be here about t = 30 min. The conductivity increases for t = 40 min ( $S_5$ ), because walls partially cracked and destroyed.

To show the effect of temperature the measurements were carried out in a chamber with dimension of  $10 \times 10 \times$  $20 \text{ cm}^3$ . One can predict that an increase of the temperature results in the increase in conductivity, seen in Fig. 6. This rising in conductivity is due to increasing electron kinetic energy, and sufficient energy for transferring electrons from valence band to conduction band, and also band gap reduces and consequently electron transferring needs less energy.

To investigate the variation of the conduction of porous silicon with temperature and frequency, an LCR multi--frequency meter was used. We measured capacitance (C) and dissipation factor (D) at 1–100 kHz frequencies



TABLE

Fig. 2. I-V characteristics of Si and PS ( $S_2$ ) at room temperature (T = 294 K).



Fig. 3. Calibration curve  $(\ln I \text{ versus } 1000/T)$  for Si.

(f) in different temperatures, so through the equation  $G = 2\pi D f C$  conduction is calculated.

Under the above considerations, the typical evolution of the porous silicon conduction G with the frequency at different temperatures is reported in Fig. 7. The curves show different electrical transport mechanisms. At frequencies higher than 10 kHz the conduction depends strongly on the frequency and is quasi-independent of the temperature. This is a typical behavior of the hopping conduction from localized states. This conduction mechanism is related to the disordered character of the porous material [21]. At low frequencies lower than 10 kHz,



Fig. 4. Calibration curve  $(\ln I \text{ versus } 1000/T)$  for PS.



Fig. 5. *I–V* characteristics of Au/PS/Si/Al structure measured at various anodization parameters.

a strong thermal activation and no frequency dependence is observed. This behavior can be attributed to the free carriers conduction through continuous paths of silicon crystallites [22].

To probe the dependance of capacitance on the temperature at different frequencies the measurements were carried out at  $10^2-10^5$  Hz frequency range.



Fig. 6. I-V characteristics of Au/PS/Si/Al structure measured at various temperatures.



Fig. 7. Conduction versus frequency at different temperatures.



Fig. 8. Capacitance of PS sample versus frequency at different temperatures.

As shown in Figs. 8 and 9, at different temperatures, for frequency100 kHz, the capacity corresponds to the geometrical value and remains constant when the conductivity increases with the frequency revealing a hopping conduction phenomena. However, capacitance decreases with the frequency. This indicates clearly the capacitive nature of porous silicon at high frequencies.



Fig. 9. Capacitance of PS sample versus temperature at 1 and 100 kHz.

# 4. Conclusion

Conduction of PS layers depends on preparation parameters such as current density, electrolyte concentration and anodization time. With increasing anodization time, increasing porosity of PS shrinks the size of silicon particles. Afterwards, cracks develop on the PS layer and small pores start to grow again, an oscillatory behaviour of the etching is observed. At frequencies more than 10 kHz conduction depends on the frequency and is independent of the temperature, this shows that at this range the dominant mechanism is hopping conduction. At low frequencies (<10 kHz) conduction depends on the temperature and is independent of the frequency. At frequencies lower than 100 kHz capacitance depends on temperature and at frequencies higher than 100 kHz it is independent of temperature. However, capacitance decreases with increasing frequency. So PS sample has a capacitive nature, and as after etching band gap and resistance of PS increase, we can use PS as a dielectric in humidity sensors.

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