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Compact Modeling for Submicron Fully Depleted SOI MOSFET's

R. Remmouche[a,b], N. Boutaoui[b] and H. Bouridah[a,b]

[a]Electronics Department, Jijel University, 18000 Jijel, Algeria

[b]LEM Laboratory, Jijel University, 18000 Jijel, Algeria

In this paper, we have developed a novel compact charge-conservative model for fully depleted silicon-on--insulator MOSFETs and implemented it in SPICE3. Our model is valid for the DC, small-signal and large-signal simulations over a wide range of temperature. Simulations made using the model, following parameter extraction, are validated by comparison with experimental data.

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1. Introduction

The thin silicon-on-insulator (SOI) CMOS technology offers numerous advantages over the bulk CMOS one, especially the reduction of some short channel effects, near subthreshold slope, increased saturation current and reduced parasitic capacitances. Moreover, SOI MOSFETs are suitable in high temperature applications since they present a low leakage current and a reduced soft error effect [1]. Hence the availability of accurate fully depleted (FD) SOI MOSFET device model is suitable to both digital and analog circuit simulation for the emerging SOI technology.

To address this need, we propose in this paper a compact model for FD SOI MOSFETs in strong inversion. In this model, a linear relationship between the surface potential and the inversion charge density is used. The drain current and the total charges are written in terms of the inversion charge densities at the drain and source ends of the channel. The explicit unified expression of the inversion charge density is applied in these equations [2, 3]. Therefore, this model can be used to calculate the drain current and all large and small signal parameters since it includes threshold voltage roll-off, parasitic source/drain resistance effect, mobility reduction due to the vertical field, carrier velocity saturation effect, drain induced conductivity enhancement (DICE), channel length modulation (CLM), drain induced barrier lowering (DIBL), floating body effect, hot carrier effect and self heating.

2. Model formalism

To reduce power consumption, supply voltage of a MOSFET has been reduced with technology scaling. The threshold voltage (V_{TH}) has also been lowered to maintain high performance. The threshold voltage of an N-channel SOI MOSFET is classically given [4] by

$$V_{TH} = V_{FB} + 2\Phi_F + q\frac{N_A x_{d\,max}}{C_{ox}}, \tag{1}$$

where $V_{FB} = -Q_{SS}/C_{ox}$ is the flat band voltage, Φ_{MS} is the work function difference between the gate and the channel, Q_{SS} is the surface state charge of the channel, C_{ox} is the front-gate capacitance, t_{ox} is the front gate oxide thickness, Φ_F is the Fermi potential, and x_{dmax} is the maximum depletion width.

To control the threshold voltage, several factors can be used. The first one is the channel concentration doping which directly affects the Fermi potential and the depletion charge of the channel. The second factor is the gate oxide thickness which represents a reverse proportion of the gate capacitance, and the third factor is related to the gate work function which has a direct control on the threshold voltage.

The expression of the drain current is evaluated for the following operation regions: cut-off region, linear region, and saturation region. The current flowing through the body of a MOSFET can be written as

$$I_{DS} = 2\mu\frac{W}{L}\int_0^{V_{ch}} Q_{inv}(y)\frac{dV_{ch}(y)}{dy}, \tag{2}$$

where μ is the carrier mobility, $Q_{inv}(y)$ is the inversion charge and $V_{ch}(y)$ is the channel potential. $Q_{inv}(y)$ represents the difference between the total charge in the body and the bulk charge.

For the linear region, and after integrating from the source ($y = 0$) to the drain ($y = L$), we get

$$I_{DS} = \frac{W\mu_{eff}C_{ox}}{2L\left(1 + \frac{\mu_{eff}V_{DS}}{2V_{sat}L}\right)} \times\left[2V_{DS}(V_{GS} - V_{TH}) - (1+\alpha)V_{DS}^2\right]. \tag{3}$$

According to the BSIMSOI 4.0 model [5], μ_{eff} is the effective carriers mobility and equals to

$$\mu_{eff} = \frac{\mu_0}{1 + (U_a + U_c V_{BS})\left(\frac{V_{GS}+2V_{TH}}{t_{ox}}\right) + U_b\left(\frac{V_{GS}+2V_{TH}}{t_{ox}}\right)^2}, \tag{4}$$

where μ_0 is the mobility in equilibrium, U_a and U_c are respectively the first and the second order mobility degradation coefficients, V_{BS} is the bulk-source voltage, and U_b is the body effect of mobility degradation.

In Eq. (3), V_{sat} is the saturation velocity and the parameter α is given by

$$\alpha = \frac{C_{\text{Si}} C_{\text{box}}}{C_{\text{ox}}(C_{\text{Si}} + C_{\text{box}})}. \tag{5}$$

C_{Si} and C_{box} are, respectively, the silicon film and the buried oxide capacitances.

When the SOI MOSFET works in weak inversion mode, the drain-source (I_{DS}) current is mainly due to the minority carriers diffusion and depends exponentially on the front-gate voltage V_{GS}

$$I_{\text{DS}} = \frac{W}{L}\mu C_{\text{ox}} \Phi_{\text{T}}^2 \exp\left(\frac{V_{\text{GS}} - V_{\text{TH}}}{n\Phi_{\text{T}}}\right) \times\left[1 - \exp\left(\frac{-V_{\text{DS}}}{n\Phi_{\text{T}}}\right)\right], \tag{6}$$

where n is a fixed parameter, Φ_{T} is the thermal potential and γ represents the influence of the body bias on the threshold voltage.

In the saturation region, the channel current is expressed as

$$I_{\text{DSAT}} = \frac{W}{L}\frac{\mu_{\text{eff}} C_{\text{ox}}}{2(1+\alpha)}(V_{\text{GS}} - V_{\text{TH}})^2. \tag{7}$$

The terminal charges are used as state variables in the circuit simulation. All the capacitances are derived from the terminal charges to ensure charge conservation as [6, 7]:

$$C_{ij} = \frac{\partial Q_i}{\partial V_j}. \tag{8}$$

3. Results and discussion

Figures 1 and 2 show the NMOS SOI threshold voltage according to the channel doping concentration and the silicon film thickness. We can observe an increase in the threshold voltage values with the increase of the channel doping density. This result can be explained by the increase of the Fermi potential and the channel depletion charge. More effort is necessary to deplete the whole channel. We can also observe that the threshold voltage does not grow up accordingly with the silicon film thickness for highly doped channel when the silicon film goes up to 50 nm because the device goes from fully depleted to partially depleted. Then the depletion charge of the channel becomes constant and the threshold voltage goes to a fixed value [8]. From Figs. 1 and 2, we can also see that the threshold voltage goes down with the increase of the silicon film thickness when the channel doping is below 2.7×10^{17} cm^{-3}. However, the threshold voltage increases with silicon film thickness when the channel doping is above 2.7×10^{17} cm^{-3}.

Figure 3 shows the variation of the threshold voltage with silicon film and gate oxide thickness. The silicon film thickness changes from 20 to 70 nm, and the gate oxide from 2 to 4 nm. It can be seen that the threshold voltage is increasing with the gate oxide thickness.

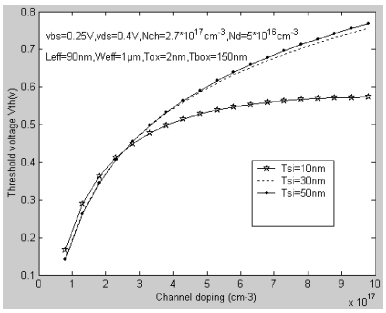

Fig. 1. Threshold voltage variation with the channel doping concentration at different silicon film thickness.

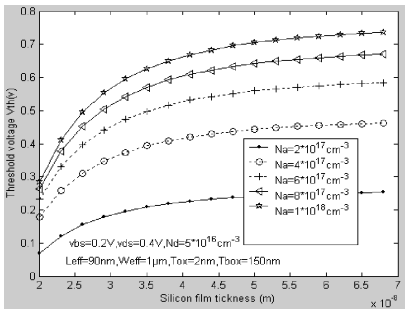

Fig. 2. Threshold voltage versus silicon film thickness at different channel doping concentration.

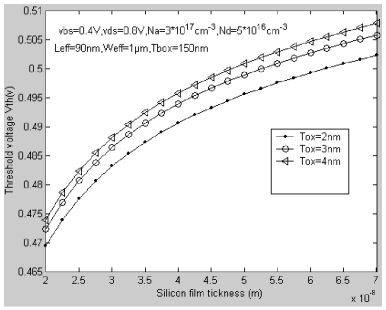

Fig. 3. Variation of the threshold voltage with the silicon film thickness for different front gate oxide thickness.

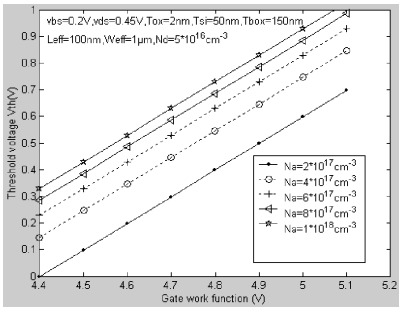

Fig. 4. Threshold voltage variation with the gate work function difference at different channel doping concentration level.

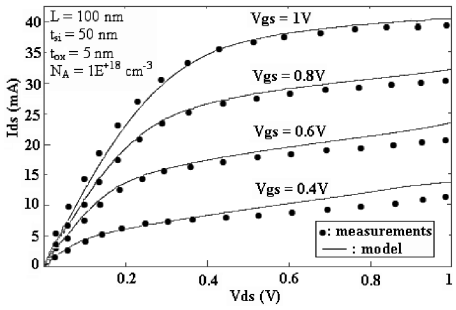

Fig. 5. Measured and simulated drain current I_{DS} as a function of drain voltage V_{DS} with L = 100 nm, W = 1 μm.

Figure 4 shows the NMOS SOI threshold voltage changing with the gate work function. The linear variation can be attributed to the fact that the gate work function affects directly the flat band voltage and then the value of the threshold voltage [9]. Thus, we can conclude that by making a change in the gate electrode work function, we can get an interesting alternative to adjust the threshold voltage.

To verify the proposed model, we present in Fig. 5 the measured and simulated (with SPICE3) I_{DS}–V_{DS} and I_{DS}–V_{GS} characteristics for a short channel NMOS SOI transistor. The channel length is 100 nm, the silicon film thickness is 50 nm, the gate oxide thickness is 5 nm and the channel doping density is 10^{18} cm^{-3}. These curves show a good agreement between the measurements and our simulation results.

4. Conclusion

In this paper, we have first found the necessity of investigating the threshold voltage control for fully depleted SOI MOSFETs. We have simulated the dependence of the threshold voltage on the channel doping concentration, the silicon film thickness, the gate oxide thickness and the gate work function. The proposed model was successfully implemented in SPICE3 and validated by comparison with experimental results. Transistors of different sizes have been characterized. The simulation results are in good agreement with measurements.

References

[1] J.P. Colinge, *Solid-State Electron.* **48**, 897 (2004).

[2] B. Iniguez, J.P. Raskin, L. Demeus, A. Nève, D. Vanhoenacker, P. Simon, M. Gouffioul, D. Flandre, *IEEE Trans. Electron Dev.* **48**, 1981 (2001).

[3] F. Djahli, S. Rahmani, R. Remmouche, *Microelectron. Eng.* **43-44**, 587 (1998).

[4] J.P. Colinge, *Silicon on Insulator Technology: Materials to VLSI*, Kluwer Academic Publishers, Boston 1997, p. 71.

[5] J.B. Roldan, F. Gamiz, J.A. Lopez-Villanueva, P. Cartujo-Cassinello, *IEEE Electron Dev. Lett.* **21**, 239 (2000).

[6] B. Iniguez, L.F. Ferreira, B. Gentinne, D. Flandre, *IEEE Trans. Electron Dev.* **43**, 568 (1996).

[7] B. Iniguez, D. Jiménez, L. Roig, H.A. Hamid, J. Pallarès, *IEEE Trans. Electron Dev.* **52**, 1868 (2005).

[8] M.J. Kumar, A. Chaudhry, H. Kumomi, *IEEE Trans. Electron Dev.* **51**, 569 (2004).

[9] G.V. Reddy, M.J. Kumar, *IEEE Trans. Nanotechnol.* **4**, 260 (2005).