High Quality Gate Insulator/GaN Interface for Enhancement-Mode Field Effect Transistor

A. Taube\textsuperscript{a,b,*}, R. Kruszka\textsuperscript{a}, M. Borysiewicz\textsuperscript{a}, S. Gieraltowska\textsuperscript{a},
E. Kamińska\textsuperscript{a} and A. Piotrowska\textsuperscript{a}

\textsuperscript{a}Institute of Electron Technology, al. Lotników 32/46, 02-668 Warsaw, Poland
\textsuperscript{b}Institute of Microelectronics and Optoelectronics, Warsaw University of Technology
Koszykowa 75, 00-662 Warsaw, Poland

\textsuperscript{c}Institute of Physics, Polish Academy of Sciences, al. Lotników 32/46, 02-668 Warsaw, Poland

The capacitance-voltage measurements were applied for characterization of the semiconductor/dielectric interface of GaN MOS capacitors with SiO\textsubscript{2} and HfO\textsubscript{2}/SiO\textsubscript{2} gate stacks. From the trapping method low density of interface traps \( (D_{it} \approx 10^{11} \text{ cm}^{-2}) \) at SiO\textsubscript{2}/GaN interface were calculated for as-deposited samples. Samples with HfO\textsubscript{2}/SiO\textsubscript{2} gate stacks have higher density of interface traps as well as higher density of mobile charge and effective charge in the dielectric layers. High quality of SiO\textsubscript{2}/GaN interface shows applicability of SiO\textsubscript{2} as a gate dielectric in GaN MOSFET transistors.

PACS: 77.55.dj, 77.22.Ch, 73.40.Qv, 81.15.Gh, 81.15.Cd

1. Introduction

Significant impact on developing new technologies for energy saving enhancement and power quality indicates necessity of progress in designing and fabrication of novel semiconductor materials and devices. Wide band gap materials such as SiC and GaN could satisfy these requirements [1]. GaN-based field effect transistors appear to be promising for application in high-temperature and high-power electronic devices due to high electron mobility and velocity as well as high critical electric field of gallium nitride. Currently, high electron mobility transistors (HEMTs) with superior characteristics have been developed [2]. Most of recently fabricated GaN-based HEMTs belong to a group of depletion-mode devices [3]. Enhancement mode operation is necessary for application of GaN-based devices in digital circuits and reduction of complexity of analog circuits. Several techniques have been developed to produce enhancement mode devices — e.g. fluorine ions shallow implantation using plasma (such as CF\textsubscript{4}) [4] or introduction of recessed-gate structure [5] in InAlN, AlN or AlGaN barrier layer. However, many of the reported threshold voltage \( (V_{th}) \) values are unacceptably low [6]. These values are insufficient to avoid malfunctions. Metal-oxide semiconductor field effect transistor (MOSFET) structure is required for achieving higher \( V_{th} \) value. Moreover, conventional HEMTs suffer from power losses due to high leakage current through the Schottky gate.

Most of GaN MOSFETs belong to the lateral devices [7, 8], however first vertical devices were also demonstrated [9, 10]. This is due to the lack of availability of good quality single crystal gallium nitride substrates. Lateral devices are mostly fabricated on GaN/sapphire substrates [7]. Compared with the silicon carbide MOSFET, gallium nitride transistors have a much better interface between the semiconductor and dielectric, and the devices with carrier mobility in the channel above 100 cm\textsuperscript{2}/(Vs) was demonstrated [11]. In these devices PECVD SiO\textsubscript{2} was used as a gate dielectric, and it was shown that high temperature annealing in nitrogen ambient greatly reduces interface states density [12].

However silicon oxide has low dielectric constant \( (\varepsilon_r = 3.9) \), which causes that 2.5 times higher electric field can be induced in the oxide than in the GaN. This may cause serious reliability problems, especially in vertical power MOSFETs [10, 13]. To overcome these problems high-\( \kappa \) dielectrics or double dielectrics stacks e.g. high-\( \kappa \)/SiO\textsubscript{2} should be used instead of SiO\textsubscript{2}. The second approach was applied successfully in silicon carbide MOS devices [13, 14]. In this paper we present the properties of SiO\textsubscript{2} and HfO\textsubscript{2}/SiO\textsubscript{2} gate stacks on gallium nitride inferred from capacitance-voltage measurements.

2. Experimental details

5 \( \mu \)m thick \( n \)-type GaN epilayers on sapphire substrate, doped to \( 2 \times 10^{16} \text{ cm}^{-3} \), were used to fabricate MOS capacitors. The samples were cleaned using the conventional RCA method followed by a 3 min dip in buffered HF. After cleaning, 10/200 nm thick titanium/
aluminum bilayer was sputter-deposited and annealed at 900°C to form ohmic contact. Two types of samples were fabricated. The first one with 30 nm thick SiO₂ layer deposited by plasma enhanced chemical vapor deposition (PECVD), and the second — with 10 nm PECVD-grown SiO₂ pedestal layer followed by DC magnetron sputtered 45 nm thick HfO₂ layer. Silicon oxide layer was deposited using SiH₄ (2% in N₂) and N₂O gases. Hafnium oxide film was reactivity sputtered from hafnium target at room temperature in O₂/Ar (70%/30%) ambient. After deposition of SiO₂, thermal annealing was performed in N₂ ambient for 30 min at temperatures from the range 800–1000°C. Finally, metal-oxide-semiconductor (MOS) capacitors were fabricated by depositing and patterning of 10 nm/200 nm thick Ti/Al electrodes. MOS capacitors was characterized by measurements of capacitance–voltage characteristic (at 1 MHz) on Agilent 1500B semiconductor parameter analyzer with Cascade Summit 12000AP probe station.

3. Results and discussion

Figure 1a shows the effect of annealing on the measured and normalized capacitance–voltage characteristic of SiO₂/GaN MOS capacitors. As we can see, due to annealing C–V characteristics were shifted towards negative voltages, which indicates increase of positive effective charge density in SiO₂ layer. Effective charge can be calculated using the following formula [15]:

\[ Q_{eff} = -C_{ox} \left( \frac{V_{FB} - \varphi_{ms}}{q} \right), \]

where \( C_{ox} \) is oxide capacitance, \( V_{FB} \) is flatband voltage and \( \varphi_{ms} \) is work function difference between gate metal and semiconductor. In case of HfO₂/SiO₂ gate stacks (Fig. 1b) C–V characteristics were shifted towards positive voltages, which is associated with the occurrence of a negative charge. Deposition of hafnium oxide changes the sign of the charge, which suggests existence of large positive charge in sputtered HfO₂ layers. Figure 2 presents hysteresis effect in C–V characteristics measured from inversion to accumulation and in the opposite direction.

As we can see in Fig. 2a, hysteresis in SiO₂/GaN capacitors is very small in comparison with HfO₂/SiO₂/GaN structures. Large hysteresis in double dielectric stack is attributed to mobile charge which is located in HfO₂ layer. Obtained results from \( V_{FB}, Q_{eff} \), and hysteresis width are presented in Table. Minimum density of effective charge and minimum hysteresis width for both type of structures are obtained for samples annealed at 900°C and as-deposited samples, respectively.

Capacitance of MIS structure in accumulation regime is equal to \( C_{ox} \). From this effective dielectric constant \( \kappa \) could be calculated. Assuming that SiO₂ dielectric constant is equal to 3.9, hafnium oxide dielectric constant was estimated to be about 15, which is comparable with results reported in literature [16].

Terman method was applied to calculate the interface state density by fitting the experimental curves at room temperature with theoretical ones [17]. The interface state density is plotted in Fig. 3. The lowest interface state density was obtained for as-deposited SiO₂/GaN samples (\( D_{it} \approx 10^{11} \text{ eV}^{-1} \text{ cm}^{-2} \)). For HfO₂/SiO₂/GaN structures the lowest \( D_{it} \) was obtained for samples with SiO₂ pedestal layer annealed at 800 and 1000°C, however these values are about one order of magnitude higher than in case of as-deposited SiO₂/GaN samples.
TABLE

Effective oxide charges and hysteresis width for SiO$_2$/GaN and HfO$_2$/SiO$_2$/GaN capacitors.

| SiO$_2$ annealing temperature | SiO$_2$/GaN | | HfO$_2$/SiO$_2$/GaN | |
|-------------------------------|-------------| | | | |
|                               | $Q_{eff}$ [cm$^2$] | Hysteresis [V] | $Q_{eff}$ [cm$^2$] | Hysteresis [V] | |
| as-deposited                  | $6.8 \times 10^{11}$ | 0.03 | $-8.3 \times 10^{11}$ | 2.13 | |
| 800 °C                        | $3.4 \times 10^{11}$ | 0.21 | $-6.4 \times 10^{11}$ | 2.55 | |
| 900 °C                        | $2.5 \times 10^{12}$ | 0.18 | $-2.6 \times 10^{12}$ | 2.56 | |
| 1000 °C                       | $4.1 \times 10^{12}$ | 0.02 | $-6.7 \times 10^{11}$ | 2.03 | |

4. Conclusions

In this paper an investigation of SiO$_2$/GaN and HfO$_2$/SiO$_2$/GaN MOS capacitors has been presented. It has been demonstrated that PECVD-grown SiO$_2$ layer on GaN creates high quality interface with interface state density of about $1 \times 10^{11}$ eV$^{-1}$ cm$^{-2}$ near conduction band edge. High temperature annealing of SiO$_2$ layer raises the density of interface states and the effective charge in the insulator. HfO$_2$/SiO$_2$ double dielectric stack has higher interface trap density and an opposite sign of effective charge compared to SiO$_2$/GaN samples. Also, hysteresis width is about one order of magnitude higher in HfO$_2$/SiO$_2$ samples. Process parameters of deposition of HfO$_2$ layer should be further optimised for GaN based devices. The low density of interface states at SiO$_2$/GaN interface will allow the use of silicon oxide gate dielectric in gallium nitride MOSFET technology.

Acknowledgments

The research was partially supported by the European Union within European Regional Development Fund, through grant Innovative Economy (POIG.01.01.02-00-108/09, “MIME”).

Sylwia Gierałtowska was supported by the European Union within European Regional Development Fund, through grant Innovative Economy (POIG.01.01.02-00-008/08).

References