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High Quality Gate Insulator/GaN Interface for Enhancement-Mode Field Effect Transistor

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The capacitance–voltage measurements were applied for characterization of the semiconductor/dielectric interface of GaN MOS capacitors with SiO_2 and HfO_2/SiO_2 gate stacks. From the Terman method low density of interface traps ($D_{it} \approx 10^{11}$ eV^{-1} cm^{-2}) at SiO_2/GaN interface was calculated for as-deposited samples. Samples with HfO_2/SiO_2 gate stacks have higher density of interface traps as well as higher density of mobile charge and effective charge in the dielectric layers. High quality of SiO_2/GaN interface shows applicability of SiO_2 as a gate dielectric in GaN MOSFET transistors.

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1. Introduction

Significant impact on developing new technologies for energy saving enhancement and power quality indicates necessity of progress in designing and fabrication of novel semiconductor materials and devices. Wide band gap materials such as SiC and GaN could satisfy these requirements [1]. GaN-based field effect transistors appear to be promising for application in high-temperature and high-power electronic devices due to high electron mobility and velocity as well as high critical electric field of gallium nitride. Currently, high electron mobility transistors (HEMTs) with superior characteristics have been developed [2]. Most of recently fabricated GaN-based HEMTs belong to a group of depletion-mode devices [3]. Enhancement mode operation is necessary for application of GaN-based devices in digital circuits and reduction of complexity of analog circuits. Several techniques have been developed to produce enhancement mode devices — e.g. fluorine ions shallow implantation using plasma (such as CF_4) [4] or introduction of recessed-gate structure [5] in InAlN, AlN or AlGaN barrier layer. However, many of the reported threshold voltage (V_{th}) values are unacceptably low [6]. These values are insufficient to avoid malfunctions. Metal-oxide semiconductor field effect transistor (MOSFET) structure is required for achieving higher V_{th} value. Moreover, conventional HEMTs suffer from power losses due to high leakage current through the Schottky gate.

Most of GaN MOSFETs belong to the lateral devices [7, 8], however first vertical devices were also demonstrated [9, 10]. This is due to the lack of availability of good quality single crystal gallium nitride substrates. Lateral devices are mostly fabricated on GaN/sapphire substrates [7]. Compared with the silicon carbide MOSFET, gallium nitride transistors have a much better interface between the semiconductor and dielectric, and the devices with carrier mobility in the channel above 100 cm^2/(Vs) was demonstrated [11]. In these devices PECVD SiO_2 was used as a gate dielectric, and it was shown that high temperature annealing in nitrogen ambient greatly reduces interface states density [12].

However silicon oxide has low dielectric constant ($\varepsilon_r = 3.9$), which causes that 2.5 times higher electric field can be induced in the oxide than in the GaN. This may cause serious reliability problems, especially in vertical power MOSFETs [10, 13]. To overcome these problems high-κ dielectrics or double dielectrics stacks e.g. high-κ/SiO_2 should be used instead of SiO_2. The second approach was applied successfully in silicon carbide MOS devices [13, 14]. In this paper we present the properties of SiO_2 and HfO_2/SiO_2 gate stacks on gallium nitride inferred from capacitance–voltage measurements.

2. Experimental details

5 μm thick n-type GaN epilayers on sapphire substrate, doped to 2×10^{16} cm^{-3}, were used to fabricate MOS capacitors. The samples were cleaned using the conventional RCA method followed by a 3 min dip in buffered HF. After cleaning, 10/200 nm thick titanium/

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aluminum bilayer was sputter-deposited and annealed at 900 °C to form ohmic contact. Two types of samples were fabricated. The first one with 30 nm thick SiO_2 layer deposited by plasma enhanced chemical vapor deposition (PECVD), and the second — with 10 nm PECVD-grown SiO_2 pedestal layer followed by DC magnetron sputtered 45 nm thick HfO_2 layer. Silicon oxide layer was deposited using SiH_4 (2% in N_2) and N_2O gases. Hafnium oxide film was reactively sputtered from hafnium target at room temperature in O_2/Ar (70%/30%) ambient. After deposition of SiO_2, thermal annealing was performed in N_2 ambient for 30 min at temperatures from the range 800–1000 °C. Finally, metal–oxide–semiconductor (MOS) capacitors were fabricated by depositing and patterning of 10 nm/200 nm thick Ti/Al electrodes. MOS capacitors was characterized by measurements of capacitance–voltage characteristic (at 1 MHz) on Agilent 1500B semiconductor parameter analyzer with Cascade Summit 12000AP probe station.

3. Results and discussion

Figure 1a shows the effect of annealing on the measured and normalized capacitance–voltage characteristic of SiO_2/GaN MOS capacitors. As we can see, due to

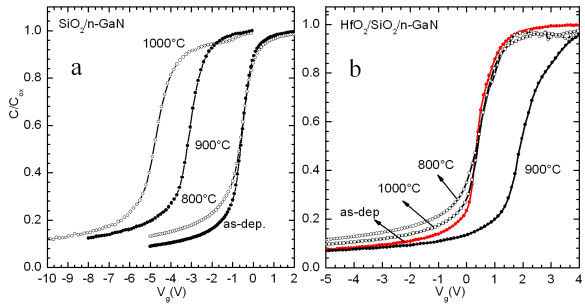

Fig. 1. (a) Normalized C–V characteristics of SiO_2/GaN MOS capacitors. (b) Normalized C–V characteristics of HfO_2/SiO_2/GaN MOS capacitors.

annealing C–V characteristics were shifted towards negative voltages, which indicates increase of positive effective charge density in SiO_2 layer. Effective charge can be calculated using the following formula [15]:

$$Q_{\text{eff}} = -C_{\text{ox}}\left(\frac{V_{\text{FB}} - \varphi_{\text{ms}}}{q}\right), \tag{1}$$

where C_{ox} is oxide capacitance, V_{FB} is flatband voltage and φ_{ms} is work function difference between gate metal and semiconductor. In case of HfO_2/SiO_2 gate stacks (Fig. 1b) C–V characteristics were shifted towards positive voltages, which is associated with the occurrence of a negative charge. Deposition of hafnium oxide changes the sign of the charge, which suggests existence of large positive charge in sputtered HfO_2 layers. Figure 2 presents hysteresis effect in C–V characteristics measured from inversion to accumulation and in the opposite direction.

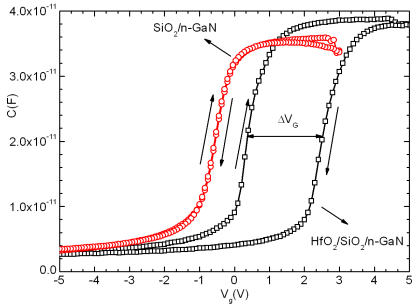

Fig. 2. Hysteresis effect in C–V characteristics of SiO_2/GaN and HfO_2/SiO_2/GaN MOS capacitors.

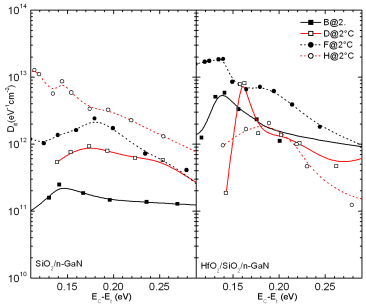

Fig. 3. Interface state density (D_{it}) of SiO_2/GaN and HfO_2/SiO_2/GaN.

As we can see in Fig. 2a, hysteresis in SiO_2/GaN capacitors is very small in comparison with HfO_2/SiO_2/GaN structures. Large hysteresis in double dielectric stack is attributed to mobile charge which is located in HfO_2 layer. Obtained results from V_{FB}, Q_{eff}, and hysteresis width are presented in Table. Minimum density of effective charge and minimum hysteresis width for both type of structures, are obtained for samples annealed in 900 °C and as-deposited samples, respectively.

Capacitance of MIS structure in accumulation regime is equal to C_{ox}. From this effective dielectric constant κ could be calculated. Assuming that SiO_2 dielectric constant is equal to 3.9, hafnium oxide dielectric constant was estimated to be about 15, which is comparable with results reported in literature [16].

Terman method was applied to calculate the interface state density by fitting the experimental curves at room temperature with theoretical ones [17]. The interface state density is plotted in Fig. 3. The lowest interface state density was obtained for as-deposited SiO_2/GaN samples ($D_{\text{it}} \approx 10^{11}$ eV^{-1} cm^{-2}). For HfO_2/SiO_2/GaN structures the lowest D_{it} was obtained for samples with SiO_2 pedestal layer annealed at 800 and 1000 °C, however these values are about one order of magnitude higher than in case of as-deposited SiO_2/GaN samples.

TABLE

Effective oxide charges and hysteresis width for SiO_2/GaN and HfO_2/SiO_2/GaN capacitors.

SiO_2 annealing temperature	SiO_2/GaN		HfO_2/SiO_2/GaN	
	Q_{eff} [cm^2]	Hysteresis [V]	Q_{eff} [cm^2]	Hysteresis [V]
as-deposited	6.8×10^{11}	0.03	-8.3×10^{11}	2.13
800 °C	3.4×10^{11}	0.21	-6.4×10^{11}	2.55
900 °C	2.5×10^{12}	0.18	-2.6×10^{12}	2.56
1000 °C	4.1×10^{12}	0.02	-6.7×10^{11}	2.03

4. Conclusions

In this paper an investigation of SiO_2/GaN and HfO_2/SiO_2/GaN MOS capacitors has been presented. It has been demonstrated that PECVD-grown SiO_2 layer on GaN creates high quality interface with interface state density of about 1×10^{11} eV^{-1} cm^{-2} near conduction band edge. High temperature annealing of SiO_2 layer raises the density of interface states and the effective charge in the insulator. HfO_2/SiO_2 double dielectric stack has higher interface trap density and an opposite sign of effective charge compared to SiO_2/GaN samples. Also, hysteresis width is about one order of magnitude higher in HfO_2/SiO_2 samples. Process parameters of deposition of HfO_2 layer should be further optimised for GaN based devices. The low density of interface states at SiO_2/GaN interface will allow the use of silicon oxide gate dielectric in gallium nitride MOSFET technology.

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