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# Native Deep-Level Defects in MBE-Grown *p*-Type CdTe

K. Olender*, T. Wosiński, A. Mąkosa, P. Dłużewski, V. Kolkovsky and G. Karczewski

Institute of Physics, Polish Academy of Sciences, al. Lotników 32/46, 02-668 Warsaw, Poland

Deep-level transient spectroscopy was used to study the defect levels in *p*-type CdTe layers grown by the molecular-beam epitaxy technique on lattice-mismatched GaAs substrates. In our measurements we have observed five hole traps. Two of the traps, displaying exponential capture kinetics, have been assigned to native point defects, the Cd vacancy and a complex formed of Cd vacancy and Te antisite, produced in the CdTe layers during their growth. The other two traps have been attributed to electronic states of threading dislocations on the ground of their logarithmic capture kinetics. The last trap, which was observed only when the investigated space charge region was close to the metal–semiconductor interface, has been ascribed to surface states.

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## 1. Introduction

Cadmium telluride in view of its wide band-gap, high average atomic number, high absorption coefficient, and high intrinsic resistivity is attractive material for X- and gamma-ray detectors, high efficiency solar cells, and nonlinear optical devices. For all the applications, identifying of electronic deep levels and their charge states in CdTe is of fundamental importance. In this paper we report results of investigations of native deep-level defects in CdTe epitaxial layers grown by the molecular-beam epitaxy (MBE) technique on lattice-mismatched GaAs substrates.

## 2. Experimental details

CdTe layers of 5 $\mu$m thickness were grown by the MBE technique, under stoichiometric conditions, on (001)-oriented $p^+$-type, Zn-doped GaAs substrates. Prior to deposition of CdTe layers, the GaAs substrate was covered with thin, 3 monolayer thick, undoped ZnTe layer to reduce the strong lattice mismatch of 14.6% between CdTe and GaAs and to stabilize the growth in the [001] direction. During the growth the CdTe layers were intentionally *p*-doped with nitrogen acceptors using an RF plasma source.

The strong lattice mismatch between CdTe layer and GaAs substrate results in the creation of a high density of misfit dislocations at the interface. The misfit dislocations generate threading dislocations, which propagate through the CdTe layer during the epitaxial growth. Their density decreases with increasing distance from the interface, as shown in the image of transmission electron microscopy (TEM) presented in Fig. 1. The very thin ZnTe layer is not recognized in the image.

The technique of deep-level transient spectroscopy (DLTS) was used to identify a set of deep electronic states

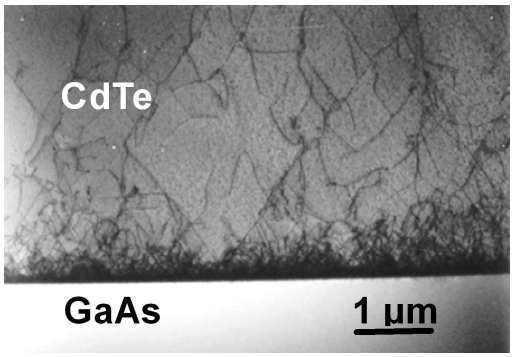


Fig. 1. Bright-field TEM image of the GaAs/CdTe:N interface in cross-section along the [110] zone axis.

in the band gap of *p*-CdTe layers employing the Schottky barriers, obtained by sputtering aluminum onto CdTe surface, freshly etched in a 2% bromine–methanol solution for 10 s. The aluminum layer was covered with gold in order to prevent oxidizing. Ohmic contacts to the samples were realized by indium soldering to the backside of the $p^+$-GaAs substrate. Room-temperature free carrier concentration in the CdTe layers was $2.4 \times 10^{16}$ cm$^{-3}$, as found from capacitance vs. voltage measurements recorded at a frequency of 1 MHz.

DLTS is a widely used, powerful and well-established technique for investigating deep band-gap states in semiconductor materials and structures. It is based on the registration of the capacitance changes of the space charge region in a Schottky or *p*–*n* junction [1]. This method provides important information about deep-level defects, like the activation energy of thermal emission of charge carriers from the levels, capture cross-sections and defect concentrations. Additionally, measurements of the kinetics for capture of charge carriers into the defect states enable to distinguish isolated point defects or impurities from extended defects, such as dislocations.

* corresponding author; e-mail: olender@ifpan.edu.pl

## 3. DLTS results

DLTS measurements, carried out in the temperature range from 90 to 400 K and under various reverse bias voltages $V_R$ and filling pulse amplitudes $V_P$, showed five

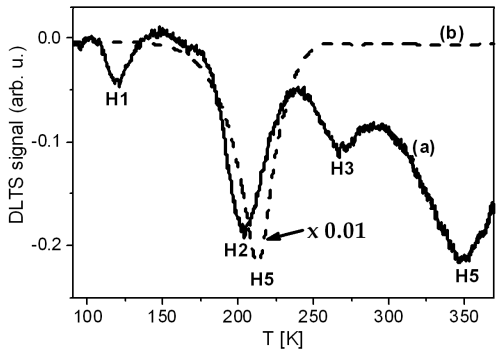


Fig. 2. DLTS spectra measured at $V_R = -3$ V and $V_P = 1.5$ V (a) and $V_R = -3$ V and $V_P = 4$ V (b) at a rate window of 43.4 $s^{-1}$, filling pulse time $t_P = 0.2$ ms.

hole traps called H1 to H5. DLTS spectra performed under the reverse bias voltage of $-3$ V and two different filling pulse amplitudes are presented in Fig. 2. The H5 trap was revealed only when the investigated space charge region of the Schottky diode was close to the metal–semiconductor interface, suggesting that the H5 trap is associated with acceptor states at the CdTe surface. The amplitude of the corresponding DLTS peak is by two orders of magnitude larger than that of the other peaks, therefore they are not visible in the spectrum (b) in Fig. 2.

Basing on temperature dependence of the DLTS spectra measured for various rate windows and constant filling pulse time, the dependence of the thermal emission rate of holes from the traps on reciprocal temperature (the Arrhenius plot) has been calculated for each trap; see Fig. 3. The straight lines have been fitted to the experimental data with the use of linear regression. The emission activation energies $E_a$ of the detected traps and their capture cross-sections $\sigma$, evaluated from the slopes of the Arrhenius plots and their intersections with the ordinate, respectively, are reported in Table.

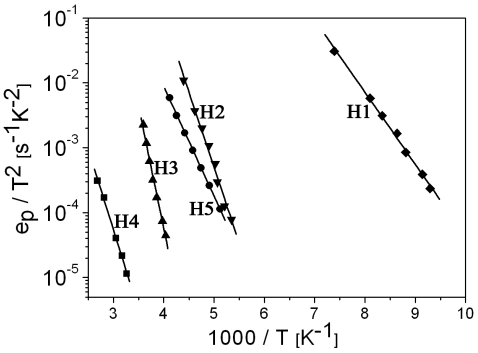


Fig. 3. Temperature dependence of the thermal emission rates (the Arrhenius plots) for the traps revealed with DLTS.

TABLE

Emission activation energies $E_a$, capture cross-sections $\sigma$ and concentrations $N_T$ of the traps revealed in the MBE-grown $p$-type CdTe:N layers and proposed defects responsible for the traps.

| Trap | $E_a$ [eV] | $\sigma$ [cm$^2$] | $N_T$ [cm$^{-3}$] | Proposed defect states |
|---|---|---|---|---|
| H1 | $E_V + 0.22$ | $3.7 \times 10^{-15}$ | $1.3 \times 10^{13}$ | dislocation core states |
| H2 | $E_V + 0.46$ | $1.5 \times 10^{-13}$ | $4.8 \times 10^{13}$ | $V_{Cd}$ (2-/-) |
| H3 | $E_V + 0.75$ | $4.8 \times 10^{-11}$ | $5.3 \times 10^{13}$ | $V_{Cd} - Te_{Cd}$complex |
| H4 | $E_V + 0.49$ | $1.1 \times 10^{-18}$ | $3.5 \times 10^{13}$ | dislocation core states |
| H5 | $E_V + 0.33$ | $3.5 \times 10^{-17}$ | – | surface states |

The capture kinetics of charge carriers at the revealed deep-level traps was measured over the wide range of the filling pulse durations from 2 $\mu$s to 20 ms. Obtained results are presented in Figs. 4 and 5. Explicit saturation of the DLTS-peak amplitude during the increase of the filling time is observed for the H2 and H3 traps (Fig. 4). They are characterized by exponential kinetics of carrier capture, which means that the observed traps originate from isolated point defects [1].

In the case of H1, H4 and H5 traps, the dependence of DLTS-peak amplitude on the filling pulse time is logarithmic (Figs. 4 and 5), suggesting that the traps are related to electronic states of extended defects [2, 3]. Such logarithmic capture kinetics results from the formation of a Coulombic barrier around the charged extended defect, whose height increases with the number of charge carriers captured at the defect. Such a capture kinetics can be described by the equation [3]:

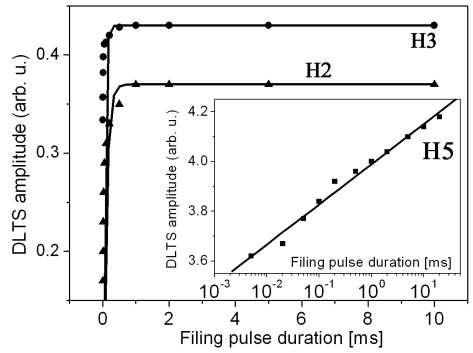


Fig. 4. Dependence of the DLTS-signal amplitude on the filling time duration for H2 and H3 traps in the main figure (linear time scale) and for the H5 trap in the inset (logarithmic time scale). The solid lines represent fittings of the exponential and logarithmic capture kinetics.

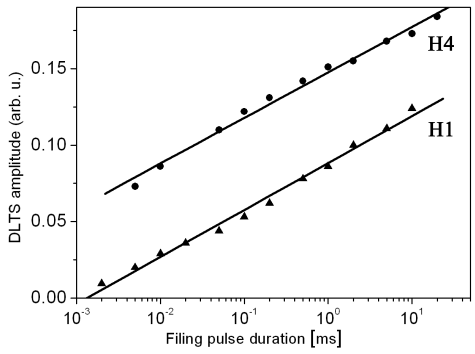


Fig. 5. Dependence of the DLTS-signal amplitude on the filling time duration for H1 and H4 traps (logarithmic time scale). The solid lines represent fittings of the logarithmic capture kinetics.

$$n_{\mathrm{T}}(t_{\mathrm{p}}) = n\sigma\langle v\rangle N_{\mathrm{T}}\tau \ln((t_{\mathrm{p}}+\tau)/\tau)\,,$$

where $n_{\mathrm{T}}$ is the concentration of the traps filled with charge carriers, $t_{\mathrm{p}}$ is a filling pulse time, $n$ is the free carrier concentration, $\langle v\rangle$ is the thermal velocity of carriers, $N_{\mathrm{T}}$ is the average trap concentration and $\tau$ is the time constant. This equation was fitted to the experimental points for the H1 and H4 traps in Fig. 5 and for the H5 traps in the inset in Fig. 4.

## 4. Discussion and conclusions

The H2 and H3 hole traps, which exhibit exponential capture kinetics, are most likely related to native point defects produced during the epitaxial growth of CdTe layers. The H2 trap, with the activation energy for hole emission of 0.46 eV, is probably the same trap, which we observed recently as a minority-carrier trap in MBE-grown $n$-type CdTe:I layers. We attributed this trap to the (2-/-) level of Cd vacancy, $\mathrm{V_{Cd}}$ [4].

The H3 trap, displaying the activation energy of 0.75 eV, is here tentatively ascribed to a complex formed of $\mathrm{V_{Cd}}$ and the Te antisite defect, $\mathrm{Te_{Cd}}$. Deep-level traps with similar activation energy as the H3 trap were observed by other groups in undoped CdTe and CdZnTe crystals [5, 6], as well as in CdTe crystals doped with Cl [6, 7], Al [8] and In [9]. Some of the authors attributed this trap to an acceptor complex involving the native $\mathrm{V_{Cd}}$ (2-/-) defect and an impurity. However, because this defect was observed in CdTe crystals doped with various elements and also in our CdTe layers grown with MBE under very clean conditions, it should be rather of native origin. The assignment of the H3 trap to the $\mathrm{V_{Cd}}$–$\mathrm{Te_{Cd}}$ complex is in agreement with previous suggestions [5] and with the results of *ab initio* calculations of its deep-level position in the band gap [10]. The $\mathrm{Te_{Cd}}$ antisite consists of a group of five neighbouring Te atoms, which might be considered as the early stage of a growing Te precipitate, very often present in CdTe crystals, and appears to complex with a vacancy in the early stages [5].

In the case of H1 and H4 traps the dependence of DLTS-signal amplitude on the filling-pulse time, observed over the range of four orders of magnitude of the time, was logarithmic. We assign these traps to the core states of threading dislocations, generated at the mismatched interface with the substrate and propagating through the CdTe layer. Segments of those dislocations intersecting the TEM foil are visible in the TEM foil are probably displayed in the micrograph of Fig. 1. Most of them display the angle of about 55° with the interface plane and the angle of about 70° between two sets of dislocations. The geometry of those dislocations suggests that they are dislocations of 60°-type lying along various ⟨011⟩ crystallographic directions at the {111} glide planes inclined at the angles of 55° with the (001) interface plane. 60°-dislocatios are the most common type of dislocations in the structure of zinc blende. This dislocations may glide under residual stress through the epitaxial layer.

Summarizing, in our DLTS investigations we revealed five hole traps in $p$-type CdTe epitaxial layers grown by the MBE technique on GaAs substrate. Basing on the obtained emission activation energies of the traps, capture kinetics and literature data, we have proposed the identification of the defects responsible for the traps. Two of the traps have been assigned to native point defects, $\mathrm{V_{Cd}}$ and complex formed of $\mathrm{V_{Cd}}$ and $\mathrm{Te_{Cd}}$, produced in the CdTe layers during their growth. Another two deep-level traps have been attributed to the core states of dislocation threading through the layers and the last one has been ascribed to surface states.

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