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Electronic Properties of Thin HfO_2 Films Fabricated by Atomic Layer Deposition on 4H-SiC

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Applicability of thin HfO_2 films as gate dielectric for SiC MOSFET transistor is reported. Layers characterisation was done by means of atomic force microscopy and scanning electron microscopy, spectroscopic ellipsometry and C–V and I–V measurements of MIS structures. High permittivity dielectric layers were deposited using atomic layer deposition. Investigation showed high value of $\kappa = 15$ and existence of high density surface states (5×10^{12} eV^{-1} cm^{-2}) on HfO_2/SiC interface. High leakage current is caused probably due to low conduction band offset between hafnium oxide and silicon carbide.

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1. Introduction

The excellent electrical and thermal properties of silicon carbide enable it to be a substrate for MOS-based devices for high-power, high-temperature and high-frequency applications. Despite ability to grow thermally oxidized SiO_2, it is questionable to repeat success of SiO_2/Si technology. Particularly, two problems arise. SiO_2 has 2.5 times lower dielectric constant than SiC, so 2.5 times higher electric field can be induced in the oxide. Moreover, interface between SiO_2 and SiC suffers from high density of surface traps [1]. To overcome those problems, relatively low-κ SiO_2 should be replaced by high-κ dielectrics (HfO_2, Al_2O_3, ZrO_2, etc.) as an alternative gate oxide [2, 3]. This paper presents our investigations on electronic properties of thin HfO_2 films deposited by atomic layer deposition (ALD) on n-type 4H-SiC epilayers. The quality of the interface between the oxide and the compound semiconductor was of particular concern.

2. Experimental details

SiC samples, consisting of 5 μm thick n-type epilayer doped to 5×10^{15} cm^{-3} grown on n-type 4H-SiC Cree Inc. substrate, were used to fabricate the MOS capacitors, and p-type Si wafers for structural and optical measurements. The wafers were cleaned using the conventional Radio Corporation of America (RCA) method followed by a 3 min dip in buffered HF. After cleaning, 200 nm thick nickel film was sputtered and annealed as backside ohmic contact. HfO_2 films, basing on our previous experience, were deposited at 135 °C in Cambridge NanoTech Savannah-100 reactor using alternating exposures of tetrakis(dimethylamino)hafnium (TDMAH) and H_2O vapour. The deposition sequence consisted of 0.04 s H_2O pulse–8 s nitrogen purge–0.02 precursor pulse–8 s nitrogen purge. After 300 cycles 45 nm thick layers were obtained. Subsequently, a layer of Cr/Au gate electrode was sputtered on top of the HfO_2. After deposition of HfO_2 films no high temperature process was performed. Finally, metal–oxide–semiconductor (MOS) capacitors were fabricated by sputtering of 10 nm/100 nm thick Cr/Au electrodes of different areas onto the HfO_2 surface.

3. Results and discussion

Scanning electron microscopy (SEM) imaging was used to measure the thickness and surface morphology of deposited samples. A picture of cross-section and surface of HfO_2 layers deposited on Si substrate is shown in Fig. 1.

Thickness was estimated to be 45.4 nm and surface was found to be smooth. Atomic force microscopy (AFM) studies confirmed smoothness of layers. Very low roughness value of 0.7 nm was measured, which provides lack of existence of the crystalline contamination in HfO_2 films. From ellipsometric measurements studies, refractive in-

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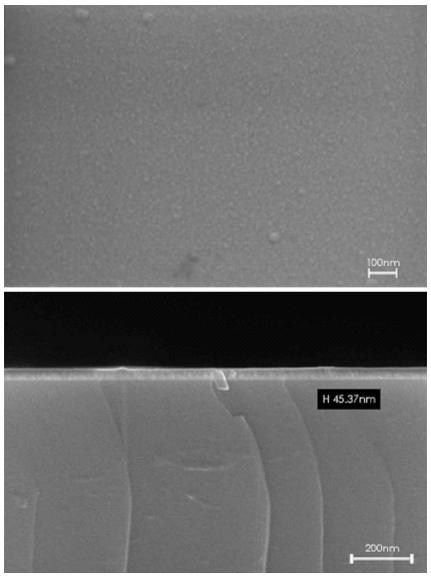

Fig. 1. SEM images of HfO_2 films on Si substrates.

dex n value of 1.91 and thickness of 43.7 nm were obtained. Extinction coefficient k value was negligible.

The current–voltage I–V characteristics were measured on Agilent B1500A Semiconductor Device Analyzer and capacitance–voltage characteristics were measured at room temperature on Agilent 4294A Precision Impedance Meter. Typical I–V plots are shown in Fig. 2.

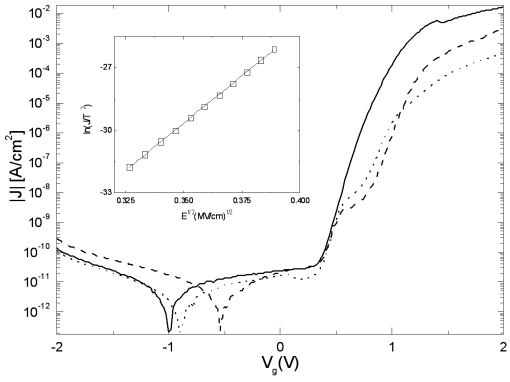

Fig. 2. I–V characteristics of HfO_2/SiC MIS capacitors. Inset presents $\ln(J/T^2)$–$E^{1/2}$ plot.

Current density in strong inversion range was very low, in accumulation range current density was few magnitudes larger. In the range 0.3 to 2 V current conduction mechanism fits very well to the Schottky emission model [4] (inset in Fig. 2) described by Eq. (1)

$$J_{\mathrm{SE}} = A^* T^2 \exp\left(\frac{-q(\Phi_{\mathrm{B}} - \sqrt{qE/4\pi\varepsilon_0 k_{\mathrm{r}}})}{kT}\right), \qquad (1)$$

where

$$A^* = \left(\frac{4\pi q m^* k^2}{h^3}\right) \qquad (2)$$

is the effective Richardson constant. Φ_{B}, m^*, k_{r}, k, and h are the Schottky barrier height, electron effective mass in insulator, dynamic electric constant, Boltzmann's constant and Planck's constant, respectively. Calculated from $\ln(J/T^2) - E^{1/2}$ plot the Schottky barrier height Φ_{B} was about 1.6 eV. We reported difference in minimum of I–V characteristic for different samples, which is probably caused by existence of charge in the insulator. Electrical breakdown field for HfO_2 layer was defined as gate voltage by which capacitors conductance on 1 MHz signal, reach 2 mS. Histogram of breakdown voltage scatter of MIS structures is shown in Fig. 3.

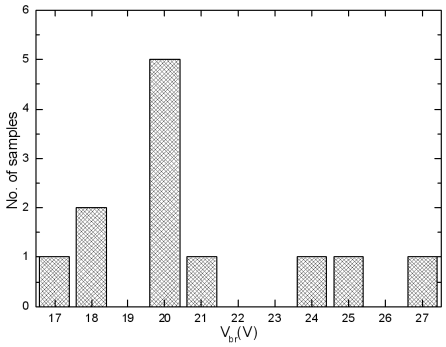

Fig. 3. Histograms of breakdown voltage scatter of MIS capacitors.

From these results average electrical breakdown field value was established to be about 5.3 MV/cm, which is comparable with results from literature [5].

Capacitance–voltage characteristics were measured in serial parallel circuit at 1 MHz. Typical C–V characteristic is shown in Fig. 4.

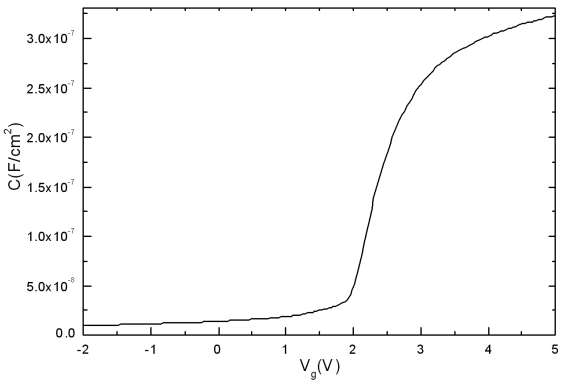

Fig. 4. Typical C–V characteristic of HfO_2/SiC MIS capacitor.

Capacitance of MIS structure in accumulation regime is equal to C_{ox}. From this effective dielectric constant κ could be calculated. For 45 nm thick HfO_2 layer, κ value

was estimated to be about 15 and equivalent oxide thickness (EOT) to be 11.7 nm. Flat-band voltage shift ΔV_{FB} for MIS capacitors was between 2.27 and 2.58 V. From these, average negative charge density at HfO_2/SiC interface was found to be around $(4.2–4.7) \times 10^{12}$ cm^{-2}.

The conductance method was applied to calculate the surface states parameters by fitting the experimental curves at room temperature with theoretical ones [6]. The times constant and interface state density are plotted in Fig. 5.

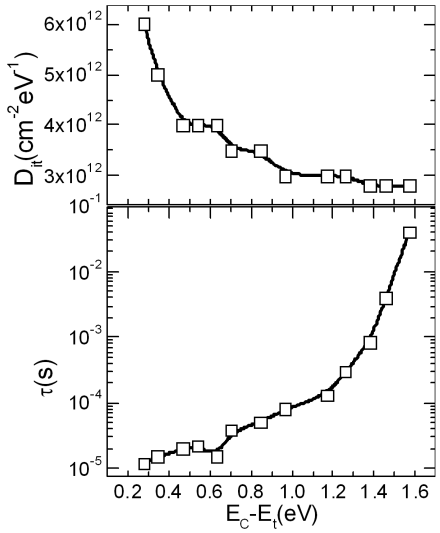

Fig. 5. Surface traps parameters (interface trap density D_{it} and time constant τ) of interface HfO_2/SiC.

The plot shows density of interface traps of 5×10^{12} eV^{-1} cm^{-2} of the energy between 0.8 and 1.6 eV below the conduction band edge. The obtained results show two types of surface traps with two different time constants. These traps have lower value of time constants and lower dependence of energetic position than in case of P_{b} centres and traps specific for SiC/SiO_2 interface [7].

4. Conclusions

Hafnium oxide films were deposited on 4H-SiC and silicon substrates by ALD at 135 °C. High dielectric constant of 15 was confirmed by C–V measurements. High leakage current (approximately 1 mA/cm^2 at 1.5 V) is probably caused by low conduction band offset between hafnium oxide and silicon carbide. It has been demonstrated that HfO_2/SiC interface suffer from high density of surface traps, which could have strong influence on electron transport in future MOSFET transistor. The reported value of 5×10^{12} eV^{-1} cm^{-2} is about one magnitude higher than in case of deposited and annealed SiO_2/4H-SiC MOS capacitors [8]. One way to prevent aforesaid problems is to introduce the pedestal layer with better potential offset between high-κ dielectric and silicon carbide, i.e. SiO_2. Ultrathin SiO_2 has potential barrier 1.1 eV higher than HfO_2.

Acknowledgments

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