

Settling Time Testing of Fast DACs

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New specialized sampling converter for signal timescale transformation and algorithm of digital signal processing for automated measurement of settling times of fast digital-to-analogue converters is represented. The new sampling device with numerically controlled oscillators allows us realization of different types of the timescale transformation. Usage of $\Sigma\Delta$ analogue-to-digital converter and first-in first-out memory allows us significant simplification of the device. The equations of timescale transformation ratio and sampling step are presented. A method using a brick-wall comb filter in frequency domain to filter measurement signal has been developed. It is shown that such filtering allows us significant reduction of noise of measurement signal. A new method and algorithm using a brick-wall comb filter and averaging of filtered signal has been developed. Results of the research of developed digital signal processing algorithm are submitted.

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1. Introduction

Fast digital-to-analogue converters (DACs) are widely used in today's electronics industry. Settling time of the output signal is one of the most important parameters characterizing speed of these DACs [1–3]. Settling time of today's 10–16 bit fast DACs is in range from several nanoseconds to several tens of nanoseconds. Therefore it is rather complex task to measure this parameter during DAC development and manufacturing quality control process [1–8].

The topic is not widely investigated and some authors [3–6] are proposing measurement techniques for 18 bit DACs with settling times up to 30 ns. In these methods specialized sampling converters are used to securing wideband oscilloscopes from being overloaded. One of the main disadvantages of such method is that settling times are measured on the screen of the oscilloscope and therefore it is not fast and requires a very high skilled operator.

Automated sampling testers were developed and implemented by authors. These testers are suitable for measurement of settling times of fast 8–12 bit DACs [2, 7, 8]. For these testers' specialized precise circuits of sampling time step shaping, compensating low-noise sampling heads [8], and methods of amplitude normalization and automatic measurement of settling times were developed and successfully implemented. In order to perform automatic measurement of settling times of 12 or more bit DACs it is necessary to convert DAC output signal with transformed timescale to digital form and to perform digital signal processing [7].

For this purpose tester with conversion of output signal, algorithm and software release of digital processing has been developed and implemented. Implementation of digital processing has enabled further reduction of influence of internal noise of sampling head and therefore increased measurement accuracy. Further investigations of the developed testers and DSP algorithm have shown that it is possible to use these testers for settling time measurement of 12–14 bit fast DACs with readout levels of 0.5 LSB (for 14 bit DACs — 0.003%) while most of the IC producers are providing settling time measurement results on 0.1% — 0.025% level of full scale for fast DACs in production.

Authors have developed and investigated a new structure of the sampling tester for measurement of dynamic parameters of fast DACs [9] using best achievements of the previous testers and extending their capabilities by use of modern element base and digital signal processing algorithms. The aim of this paper is to present a newly developed and investigated block diagram of DAC dynamic parameter measurement tester and digital signal processing method of measurement signal.

2. Block diagram

One of the methods for further reduction of tester's internal noise level and for improvement of efficiency of digital signal processing algorithms without increasing analysis duration is to develop a new specialized sampling tester. Such tester should incorporate simple circuit of formation of sampling step and simplified hardware processing of signal after timescale transformation.

Therefore circuit of sample step formation should have flexibility ensuring different timescale transformation methods: serial sampling, backward sampling, sam-

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pling on single point and possibility for flexible change of sampling step.

Compensating sampling converters with peak detection and two quartz oscillators used earlier has shown very good metrological characteristics while being comparably simple [5–8]. These converters have low noise levels ensured by the compensating structure and high transfer coefficient. Such features ensure lower amplification needs and thus reduces amplification of its internal noise. Nevertheless these converters have limited possibilities to change sampling step and therefore cannot be used for implementation of different timescale transformation methods directly.

Complementing possibilities given by numerically controlled oscillator (NCO) with modern relatively fast $\Sigma\Delta$ analogue-to-digital converters (ADCs) it is possible to simplify circuit of processing of signal after timescale transformation considerably. Speed of ADC is related to transformation factor of the sampling converter and speed of DAC under test [8].

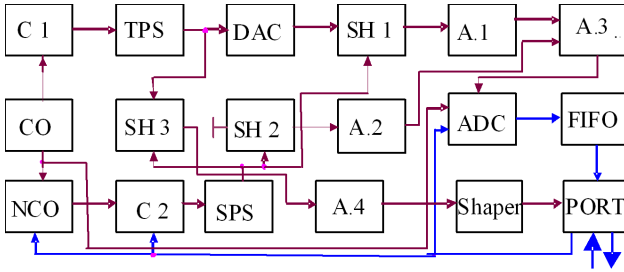


Fig. 1. Block diagram of the tester for measurement of dynamic parameters of fast multibit DACs. DAC — DAC on the test; C1, C2 — frequency dividers; CO — quartz oscillator; NCO — numerically controlled oscillator; SH1, SH2, SH3 — sampling heads; TPS — test pulse shaper, SPS — sampling pulse shaper, A1–A4 — amplifiers; ADC — analogue-digital converter; Com — commutator; PORT — port to connect PC; FIFO — data memory — first input first output.

Taking into account the aforementioned statements block diagram of a new tester for measurement of settling times of fast DACs has been developed (Fig. 1) [9, 10].

2.1. Description of operation

Output signal of quartz oscillator CO is sent to test pulse shaper TPS through frequency divider C1. TPS is producing DACs test pulses of strictly defined parameters — frequency, front times, U_{TPS}^1 and U_{TPS}^0 readout levels. Frequency of test pulses is equal to

$$f_{\text{TPS}} = \frac{f_{\text{CO}}}{p_1}, \quad (1)$$

where f_{CO} — output frequency of quartz oscillator, p_1 — division ratio of frequency divider C1.

Frequency of NCO output signal is equal to

$$f_{\text{NCO}} = \frac{6r f_{\text{CO}}}{2^{n_n}}, \quad (2)$$

where r — decimal n_n bit frequency set word.

Therefore frequency of NCO output signal is controlled by changing frequency set word r . For example for AD9851 NCO IC frequency set is possible in 0.06 Hz steps ($n_n = 32$ bit). NCO output frequency can be set so the frequency of SPS be equal to (a) TPS output frequency (thus ensuring sampling on single point); (b) lower than TPS output frequency (thus setting serial sampling); (c) higher than TPS output frequency (setting serial backwards sampling). At the same time by changing of control word r it is possible to set different phase of output signal (that is delay of output signal).

Desired frequency for the sampling pulse shaper is gained by using frequency divider C2 with divider factor p . C2 is realised as ordinary pulse counter with initial value setup. Therefore it is possible to manipulate delay in large scale by setting initial value to the counter. In this case phase control code sent to NCO after divider C2 would change output signal phase by $2\phi/p$. It is possible to set delay with the step

$$t_r = \frac{2\pi}{2^{n_f} p f_{\text{NCO}}}. \quad (3)$$

t_r is equal to $0.2/16 = 12.5$ ps when $p = 16$ and $n_f = 12$ bits which is convenient in most of the cases. It is still possible to increase output frequency of NCO and p and further reduce value of t_r .

2.2. timescale transformation and sampling step

Output pulses of the divider C2 are sent to sample pulse shaper. Short sampling pulses are produced here and sent to sample heads SH1–SH3.

Output signal from DAC on the test is sent to second input of sampling head SH1. Second input of sampling head SH2 is connecting to ground wire. Signal from test impulse shaper TPS is sent to second input of sampling head SH3. TPS output signals are also sent to all inputs of DAC on test and therefore output current (or voltage) of the DAC is changing from a minimum to a maximum value.

In case output frequency of TPS ($f_{\text{TPS}} = f_{\text{CO}}/p_1$, where p_1 — division factor of divider C1) is higher than output frequency of SPS

$$f_{\text{SPS}} = \frac{6r f_{\text{CO}}}{p 2^{n_n}}, \quad (4)$$

serial sampling mode is set. In this case signal timescale transformation and sampling step are

$$q = \frac{f_{\text{TPS}}}{f_{\text{TPS}} - f_{\text{SPS}}} = \frac{2^{n_n} p}{2^{n_n} p - 6rc}, \quad (5)$$

$$\Delta t = \frac{f_{\text{TPS}} - f_{\text{SPS}}}{f_{\text{TPS}}^2} = \frac{2^{n_n} cp - 6rc^2}{2^{n_n} p f_{\text{CO}}}. \quad (6)$$

In case f_{SPS} is set higher than f_{TPS} then backward sampling mode is set and timescale transformation and sampling step is set by (5) and (6). In this case signal with transformed timescale will be propagated from its falling edge to the rising edge.

In both cases outputs of the sampling head SH1 is output signal of DAC on the test with transformed timescale and output of sampling head SH3 is the output signal of TPS with transformed timescale. These signals are amplified by amplifiers A.1–A.4. Output signal of A.1 and A.2 are sent to A.3 and output signal of A.4 is sent to shaper. Output signal of A.3 (output of compensatory sampling head) is sent to ADC.

In order to measure dynamic parameters of 12-bit DACs it is necessary to use not less than 16 to 18-bit ADCs [7]. Therefore fast 24-bit $\Sigma\Delta$ ADC is selected for implementation. Digital code of the momentary values of input signal converted by ADC is stored in first-in first-out (FIFO) memory module. This module should have 24-bit word and clock speed not less than sampling frequency of ADC.

FIFO memory module is connected to PC through PORT interface (e.g. USB or specialized interface board) and further measurement actions are taken using digital signal processing on the PC.

In order to perform digital signal processing and further measurements it is necessary to establish main parameters of the numeric array obtained from the converter's FIFO memory module and ADC: DAC LSB value represented in number of ADC bits and the duration between two discrete values of ADC output signal.

The duration between two discrete values is equal to $1/f_{CO}$, if signal of quartz oscillator CO is set as the clock signal for ADC. Then time between two discrete values converted to real DAC time before timescale transformation is

$$t_d = \frac{1}{f_{COq}}. \quad (7)$$

Least significant bit of DAC under test represented in number of ADC bits is

$$k_{MRS} = \frac{2^{n-m} k_k U_{DAC}}{U_{ADC}}, \quad (8)$$

where U_{DAC} — scale of DAC under test output voltage; U_{ADC} — scale of ADC input voltage; m — number of bits DAC under test; n — number of bits ADC; $k_k = k_m k_s$, k_m — transfer factor of mixer; k_s — total gain of all amplifiers.

In order to record all the periods of DAC on the test it is necessary to ensure that the capacity of FIFO memory is not less than

$$k = \frac{q f_{ASK}}{f_{TPS}} = \frac{2^{n_n} p^2}{2^{n_n} p - 6rc}. \quad (9)$$

One period of a test signal of DAC under investigation stored in FIFO is sent through the PORT to PC.

3. Filtering of measurement signal

Magnitude readout levels of DAC under test settling time measurement are set to a very low voltage (tens of microvolt) difference to the settled magnitude level voltage [7]. Therefore the filter to be developed should

be capable to eliminate noise in the specified frequency range but at the same time it should not influence the test signal anyhow. This means that the pass band characteristic of the filter should be absolutely flat. Even fractional distortions of test signal would make settling time measurement impossible.

One realization of digitized real test signal of DAC under test has discrete spectrum that is spread over the frequency axis in steps [11]:

$$\omega_s = \frac{2\pi}{N}, \quad (10)$$

where N — number of samples of test signal.

In this case harmonics of the digitized test signal and internal noise that are digitized in the same device are overlapping and filtering of such signal by using filters is difficult.

Typically testers of DAC settling time with digital signal processing [7] are performing digitalization of n_r realizations of test signal where major part of the test signal is remaining basically the same but the internal noise of each realization is different due to random nature of noise sources. It is proposed to unify these n_r realizations into uniform signal of periodic test pulses and to obtain pseudo-periodic test signal.

In case limited number of n_r periods of test signal are digitized and pseudo-periodic series are generated the sine spectral components will have: first — n_r periods, third — $3n_r$ periods, fifth — $5n_r$ periods and so on and the sine wave with limited length is written as

$$u_s(m_i) = \begin{cases} \sin(2\pi m_i/M), & \text{when } |m_i| < \frac{n_i}{2}, \\ 0, & \text{when } |m_i| > \frac{n_i}{2}, \end{cases} \quad (11)$$

where n_i — number of periods of sine wave, m_i — discrete value of sine signal.

Spectrum of such sine wave signal containing n_i periods is [11]:

$$G_t = \frac{f_{0i}}{\pi(f_{0i}^2 - f^2)} \sin \frac{\pi n_i f}{2F}. \quad (12)$$

Number of periods n_i is increasing for each spectral component of rectangular pseudo-periodic signal: for first it is $1n_r$ period, third — $3n_r$ periods, fifth — $5n_r$ and so on. As it is seen from (12) each harmonic component of higher frequency of rectangular pseudo-periodic signal is narrower than previous (Fig. 2). Also it is obvious that for number of periods of test signal $n_r \rightarrow \infty$ only central band components at $f_0, 3f_0, 5f_0$ are left in the spectrum of a signal.

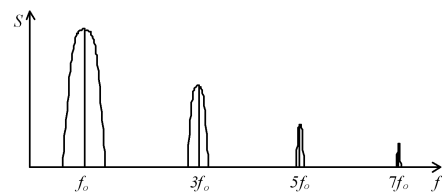


Fig. 2. Magnitude spectrum of a pseudo-periodic signal.

In case of a digital measurement signals of DAC under test it is not possible to form a full periodic signal and therefore pseudo-periodic signal has side harmonic components spaced around main harmonic components (Fig. 2). Increasing number of periods of pseudo-periodic sequence would result in increasing magnitude of the main harmonic components at f_0 , $3f_0$, $5f_0$ and narrowing side harmonic components spaced around main components. Vice versa decreasing number of periods in pseudo-periodic sequence of test signal would decrease magnitude of the main spectral components and side harmonic components will be spaced broader around main spectral components. In case number of periods of test signal $n_r \rightarrow 1$ spectrum of the sequence would become more and more similar to continuous spectrum of one realization of the measurement signal with $n_r = 1$.

Having this in mind the idea is to implement a brick-wall comb filter (further — comb filter) in frequency domain that has an ideal pass band at every harmonic f_0 area of the measurement signal and an ideal stop band at every other frequency of the measurement signal spectrum. Such filter cannot be implemented in real-time systems as it has an unlimited impulse response characteristic. Nevertheless measurement of settling time is a controlled environment where the test pulses can be generated as many times as it is necessary and therefore it is possible to process the measurement signal in non-real-time environment making a post-processing of the measurement signal.

Nevertheless it is necessary to establish conditions for filtering side harmonic components that are spaced around central harmonic components.

The proposed comb filter constructed as aforementioned will not distort a finite number of periods of pseudo-periodic signal in several cases:

(a) In case filter is constructed so that the passband includes all side harmonic components around each central harmonic (components are not set to 0 value). As aforementioned each higher central harmonic has narrower side harmonics and therefore the comb filter passband blocks needs to be constructed narrower accordingly. Transfer function of such filter is represented as

$$H(f) = \begin{cases} 1, & \text{when } mf_{s\min} < f < mf_{s\max}, \\ 0, & \text{elsewhere,} \end{cases} \quad (13)$$

where $f_{s\min}$ and $f_{s\max}$ are minimum and maximum frequency components around certain central spectral component mf_0 .

In this case after filtering of the signal in frequency domain and inverse fast Fourier transform (FFT) the resulting pseudo-periodic signal will not be distorted no matter how many spectral blocks m around central spectral components mf_0 are filtered. Nevertheless filtering efficiency is not very high as more spectral components of noise are lying in passband of the filter especially in lower frequencies where passbands of the filter are wider.

(b) In case a pseudo-periodic sequence is constructed of higher number of test signal realizations side harmonic

components around central frequencies mf_0 are narrow ($f_{s\min} - f_{s\max} \rightarrow 0$) and magnitude of these components is relatively low. Investigations have shown that constructing a pseudo-periodic sequence of 100 realizations of test signal even magnitudes of first side spectral components around f_0 ($f_0 - 1$ and $f_0 + 1$) are only 5% of magnitude of central component f_0 . Magnitude values of other side components are neglectively low. In this case the comb filter can be constructed to have passbands only at central spectral components of the pseudo-periodic sequence — mf_0 :

$$H(f) = \begin{cases} 1, & \text{when } f = mf_0 \text{ and } f < m_{f\max}f_0, \\ 0, & \text{elsewhere.} \end{cases} \quad (14)$$

In this case after filtering of the test sequence in frequency domain and inverse FFT the resulting pseudo-periodic signal will not be distorted no matter how many spectral blocks m around central spectral components mf_0 are filtered (filtered spectral blocks till $m_{f\max}$).

Filtering efficiency is significantly higher in this case as most of the noise spectral components are filtered and only spectral components of the noise that are equal to the filtered m central spectral components of the signal at frequencies $f = mf_0$ and noise at non-filtered area higher than $m_{f\max}f_0$ are in the passband of the filter.

(c) In case comb filter is filtering absolutely all spectral blocks that are not equal to central harmonics mf_0 in the whole spectrum of the signal, and the passband is only limited to frequencies that are equal to mf_0 :

$$H(f) = \begin{cases} 1, & \text{when } f = mf_0, \\ 0, & \text{elsewhere} \end{cases} \quad (15)$$

After filtering in frequency domain and inverse FFT a fully periodic sequence of the filtered signal is obtained as an output. All periods of this signal are equal.

In this case highest filtering efficiency is gained as all noise spectral components are filtered and only spectral components of the noise that are equal to the central spectral components of the signal at frequencies $f = mf_0$ are in the passband of the filter. It is obvious that such filtering can be implemented only in case spectrum of test signal is finite.

Spectrum of output signal of the compensating sampling converter is finite as the passband is limited by elements of the converter and the Nyquist frequency of ADC.

By digitalization and recording to the FIFO memory of n_r realizations of test signal forming pseudo-periodic series of test signals, internal noise of sampling head are digitized together. Sum of the pseudo-periodic test signal and a low frequency sine wave, simulating single component of $1/f$ noise is shown in Fig. 3a and a spectrum of such signal in Fig. 3b. It is seen that the spectrum of low frequency internal noise of the sampling head can be distinguished from the spectrum of the test signal.

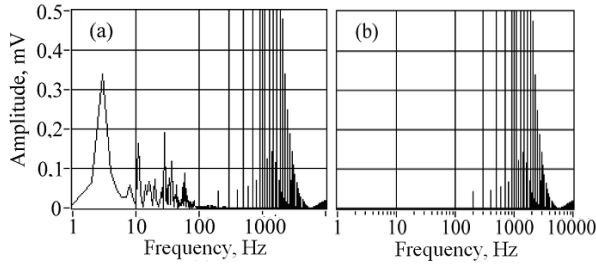


Fig. 3. Magnitude spectrum of the pseudo-periodic test signal and a low-frequency internal noise (a) and magnitude spectrum of this signal after brick-wall comb filter (b).

For this reason the pseudo-periodic testing signal is converted to a frequency domain by using FFT. After that all the spectral components differing from the main test signal spectral components (e.g. 100, 200, 300 ...) are blocked (set to $m_i = 0 + 0j$ values). Therefore major spectral components of the noise, those whose frequencies are not equal to the frequencies of the test signal, are eliminated from the resulting spectrum. The resulting spectrum is converted back to the time domain by using an inverse FFT. The output of the ideal brick-wall comb filter is the same but the periodic test signal with significantly lower level of internal noise.

Functioning of the developed digital comb filter has been tested using LabView[®]. Internal noise were simulated by (a) using sine wave of f_{i1} frequency, and initial phase of which for each test signal realization is set randomly by using continuous uniform distribution from 0 to 360° and (b) standard white noise. The noise signal is added to the ideal test signal realization. Pseudo-periodic test signal array was formed using from 10 to 100 signal realizations. Spectrum of the pseudo-periodic test signal is shown in Fig. 3a. Analysis of the filtered digital pseudo-periodic test signal with noise has shown that spectral components of the noise signal are absent or appear only because of non-ideal periodic manner of the signal in the low-frequency range (up to 80 Hz) where internal noise spectral components are most intensive (Fig. 3b). Inverse FFT was performed on the resulting spectrum to get result test signal after filtering in the time domain. Filter input noise (unfiltered) and filter output (filtered) noise intensity is shown in Fig. 4. Apparently from Fig. 4, the digital comb filter reduces intensity of the noise up to 10 times. It is seen that the developed digital filter has not influenced the testing signal and the error generated by the internal noise has reduced significantly.

Therefore 100 realizations of test signal are enough to form a pseudo-periodic test signal and the resulting harmonic components are narrow enough to prevent distortion of output signal when applying comb filter.

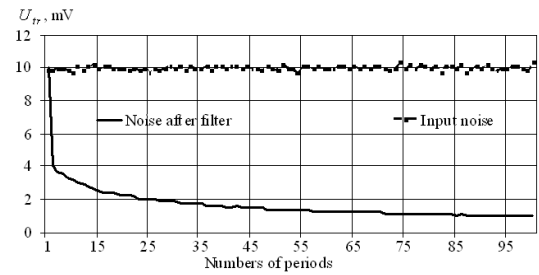


Fig. 4. Intensity of a white noise on an input and an output of the digital brick-wall comb filter.

4. Complex algorithmus of digital signal processing

Investigations of the filtering results have shown that the resulting signal has residual noise components (those that have spectrum components equal to the periodic signal spectral components) and that these cannot be reduced by averaging between periods of test sequence. Analysis has shown that the noise components have the same magnitude and phase values at each period of the test sequence (noise became periodic after filtering) and therefore averaging has no effect on the noise reduction.

Nevertheless additional set of pseudo-periodic test signals would result in different periodic noise after filtering (Fig. 5). Therefore it has been decided to filter n_i pseudo-periodic sequences each containing of n periods of test signals and then take one period from each of resulting filtered sequences and perform averaging (Fig. 6).

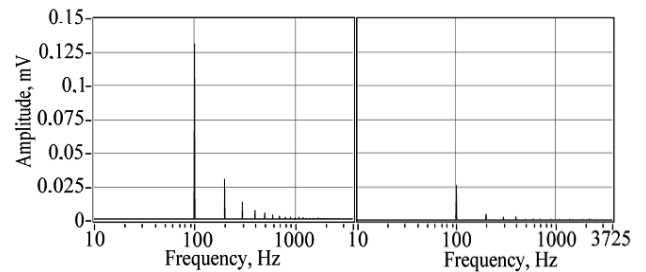


Fig. 5. Spectra of two different series of noise on an output of the comb filter.

An investigation of such algorithm using LabView[®] has shown that the residual noise are reduced effectively by this method. As it is shown in Fig. 7 by using all represented means it is possible to the reduce noise up to 100 times.

By using the represented filter and the averaging algorithm a digital processing of test signal and settling time measurement algorithm has been developed and a LabView[®] program for implementing such algorithm for measurement of settling time of DAC has been developed and investigated.

Investigations have shown that the algorithm implementing digital filtering using comb filter and averaging

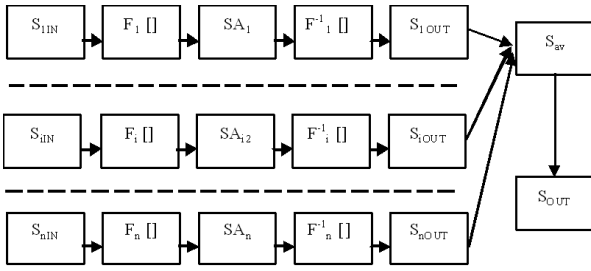


Fig. 6. Block diagram of the designed digital comb filter: $S_{1IN}, S_{iIN}, \dots, S_{nIN}$ — n -th realization input signals, $S_{1OUT}, S_{iOUT}, \dots, S_{nOUT}$ — n -th realization output signals; $F[\cdot], F^{-1}[\cdot]$ — blocks of direct and inverse Fourier transformation; SA — spectra separation block, S_{av} — averaged signal; S_{OUT} — output signals.

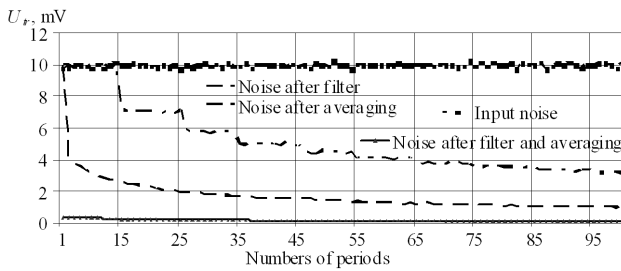


Fig. 7. The level of noises after digital signal averaging, filtering or filtering and averaging depending on the number of signal periods.

of the filtered signals has reduced influence of the internal noise of the converter to results of measurement of DAC settling time up to 60 times — Fig. 8.

5. Conclusions

1. A structure of the new automatic sampling device for measurement of dynamic parameters of fast DACs has been developed. By using a NCO, $\Sigma\Delta$ ADC and FIFO memory it is possible to simplify the device significantly by expanding functional features of the device and to introduce different types of sampling methods on one device.

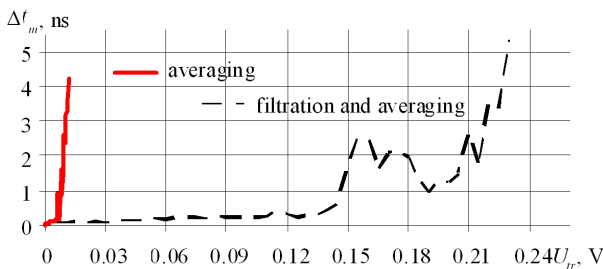


Fig. 8. Settling time testing deviations Δt_m dependence from noise voltage U_{tr} .

2. Equations of the transformation factor the sampling step and calculation of the settling time parameters of the new device were deduced.
3. The structure of the developed new sampling device can be implemented for measurement of dynamic parameters of different fast circuits, such as op-amps, gates, latches, registers, counters, etc.
4. Spectrum components of a one period of the DAC test signal and internal noise of sampling head are overlapping. Therefore it is not possible to filter noise and remove errors generated by internal noise from settling time measurement result.
5. Combining n_r realizations of the test signal with random internal noise and setting periodization parameters right it is possible to get a pseudo-periodic test signal where the test signal spectral components are separated from the random internal noise. This makes partial filtering of the test signal feasible.
6. A brick-wall comb digital filter in frequency domain has been implemented for filtering of the low-frequency internal noise while keeping the test signal not distorted. Modeling of the process has shown that the filter developed is effectively reducing low-frequency internal noise of the sampling head and white noise.
7. It has been established that signal after comb filter is fully periodic including noise components and therefore it is not possible to reduce the noise by averaging between periods of the same test sequence.
8. Algorithm for filtering n_i pseudo-periodic sequences each containing of n_r periods of the test signals and then taking one period from each of the resulting filtered sequences and performing averaging is proposed and investigated.
9. It is established that implementation of all means of digital signal processing including comb filter and averaging algorithm reduces noise level up to 100 times.
10. LabView[®] program implementing all the represented means of digital signal processing and settling time measurement has been developed and investigated. Modeling has shown that the influence of the internal noise of the sampling converter to the results of the settling time measurement of DACs is reduced by the proposed algorithm up to 60 times.

A developed method of implementation of the brick-wall comb digital filter can be used to filter other digital signals. It can be used when it is possible to get number of comparably equal test signal realizations influenced by noise and when it is possible to build pseudo-random

digitalized test signal series with right parameters to separate spectral components of test signal and noise.

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