

The Fast Differential Amplifier-Based Integrated Circuit Yield Analysis Technique

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The fast differential amplifier-based integrated circuit yield analysis technique, which enables determining the interrelation between the integrated circuit yield and dimensions of circuit elements, has been presented. The technique is based on the common use of experimental statistical analysis and statistical modeling as well as on the introduction of the concept of the integrated circuit intermediate parameters. The results of yield analysis of the concrete integrated circuit based on the differential amplifiers are presented.

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1. Introduction

Most of analogue integrated circuits (IC), e.g. comparators, operational amplifiers, analog-to-digital converters, are based on the differential amplifiers. The continuous efforts to increase the speed of these ICs require reducing the dimensions of elements. Therefore, the relative dispersion of element (transistors and resistors) dimensions increases and, because of this, the dispersion of IC parameters rises as well. This phenomenon may significantly reduce such a fundamental characteristic of IC as yield, which determines the cost of IC. Therefore, during the development of IC it is desirable to predict the yield and determine the ways for the yield increment by the variation of dimensions of elements [1]. This problem can be solved only by means of statistical analysis.

The value of IC yield at a given process technology level is determined by the IC layout (the set of element dimensions). Consequently, statistical analysis should relate the yield of ICs to the element dimensions. Parametric yield (Y_p) and catastrophic yield (Y_c) compose IC yield. Y_p is determined by dispersions of IC parameters during fabrication process. Y_c is determined by catastrophic failure caused by defects on the IC chip area.

The values of parameters of analog ICs are sensitive to dispersions of parameters of elements (transistors, resistors and others). Therefore, the yield of analog ICs (especially of small-scale integration) is mainly determined by Y_p and strongly depends on the dimensions of elements. Because of this, it is important to have at hand the interrelations between the Y_p and dimensions of elements to design an optimal IC layout for a given process technology level by yield maximum criteria. The process technology level is characterized by the minimal dimension, which can be guaranteed by the lithography during the IC fabrication process.

Theoretically, the IC model formed on the basis of physical — dimensional models of the elements could be used to determine Y_p . The distributions of IC parameters could be simulated by the Monte Carlo method with the help of such a model, knowing the probabilistic characteristics of the model parameters. However, such technique of ICs statistical analysis is difficult and even impossible to realize due to circuit model complexity.

In this work we would like to suggest the statistical analysis technique of analog ICs free from the shortcomings discussed above. This technique enables us to determine the interrelations between Y_p and dimensions of IC elements.

2. Yield analysis technique

The suggested technique enables us to determine the interrelations between Y_p and dimensions of elements (x). The idea is based on the common use of experimental statistical analysis (ESA) and statistical modeling (SM) and on the introduction of the concept of the IC intermediate parameters (IP). Due to IP appearance, the problem of IC statistical analysis in the suggested technique is divided into two more simple ones. The first of them is solved by ESA, the second one — with the help of SM. Such division considerably simplifies the problem of the IC statistical analysis and makes its solution workable at the stage of the IC design.

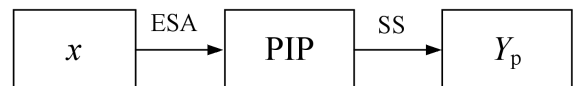


Fig. 1. The IC parametric yield analysis technique.

IC analysis in the suggested technique is carried out according to the following scheme (Fig. 1). The interrelations between x and IP probabilistic characteristics (PIP) are determined using the ESA of test structures

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consisting of IC elements with various dimensions. SM follows the Monte Carlo method on the basis of PIP and on the circuit mathematical model. Distributions of IC parameters are a result of SM. Y_p is determined on the basis of distributions knowing the limitations on IC parameters. The complexity of ESA and SM depends on IP. The parameters of electrical models of IC elements are most convenient to use as IP. In this case, we need an electrical model of IC based on electrical models of elements, on the one hand, and experimental dependences of probabilistic characteristics of elements parameters on element dimensions, on the other hand. In the suggested technique, the empirical or physical models of elements can be used. However, it is necessary that parameters of models would be measurable, i.e. it would be possible experimentally to determine the PIP dependences on x . Additionally, the models of elements should allow us to create a sufficiently simple and adequate IC model, which relates IP with IC parameters.

Taking into consideration Y_c , the total yield per wafer Y_T can be determined by the following expression:

$$Y_T = (Y_p Y_c S_w) / S_c, \quad (1)$$

where S_w is the efficient area of a wafer, S_c is the IC chip area. It is necessary to stress that Y_c and S_c depend on x and this fact must be taken into the consideration.

Generally, the statistical optimization problem should be solved. The aim of this optimization is to select the IC element dimensions values $x_1 = X_1$, $x_2 = X_2$, ..., $x_k = X_k$ from the Q region of physically possible values, at which

$$Y_T(X_1, X_2, \dots, X_k) = \max_{x_i \in Q, i=1,2,\dots,k} Y_T(x_1, x_2, \dots, x_k). \quad (2)$$

3. Yield analysis of the differential amplifiers IC

Let us apply the suggested yield analysis technique for the IC composed of four identical differential amplifiers based on bipolar junction transistors. The circuit diagram of a differential amplifier is given in Fig. 2.

The aim of the analysis is to determine the optimal dimensions of elements for the given level of IC process technology by Y_T maximum criteria. The input offset voltages $U_{OS1} \div U_{OS4}$ of the differential amplifiers were the parameters of IC. The problem was solved taking into account the condition that the layouts of all differential amplifiers are the same. The values of $U_{OS1} \div U_{OS4}$ are not sensitive to dispersion of parameters of transistors V3, V8 and resistors R3, R10. Therefore, the dimensions of V3, V8, R3, R10 are considered to be fixed. The arms of differential amplifiers must be symmetric. Consequently, the layouts of V1 and V2, R1 and R2, V4 and V5, R4 and R6, R5 and R7, V6 and V7, R8 and R9 must be the same.

Let us use the parameters of electrical models of transistors and resistance of resistors as IP for discussed IC. During the measurement of U_{OS} of differential amplifiers the transistors operate in the forward active mode at

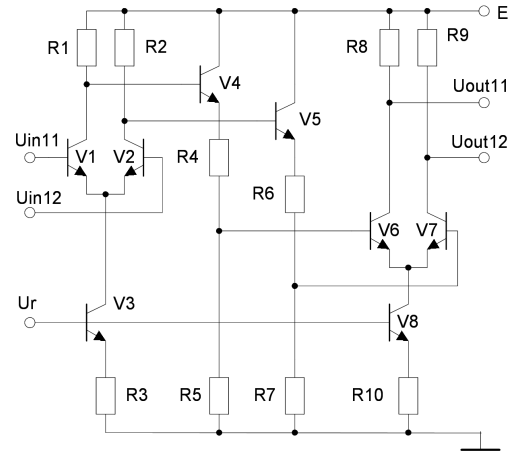


Fig. 2. Differential amplifier.

the fixed emitter current. The following empirical linear transistor model can be used for creating an equation for calculation of U_{OS} of a differential amplifier:

$$I_B = (U_{BE} - V_{Be}) / r_b, \quad I_K = \beta I_B, \quad (3)$$

where I_B is the base current, I_K is the collector current, U_{BE} is the voltage applied across the base-emitter and V_{Be} , β , r_b are the parameters of the empirical transistor model that are measured experimentally at a fixed transistor operating point, at which the U_{OS} measurement is provided.

Parameters of transistors V_{Be} , β , r_b and resistance R of resistors are used as IP. The IC model binding IP with $U_{OS1} \div U_{OS4}$ was created on the basis of a transistor model (3). The dependences of PIP on dimensions of elements were determined by ESA. It was obtained that the hypothesis concerning the normal distributions of transistor parameters and the resistor resistance can be accepted.

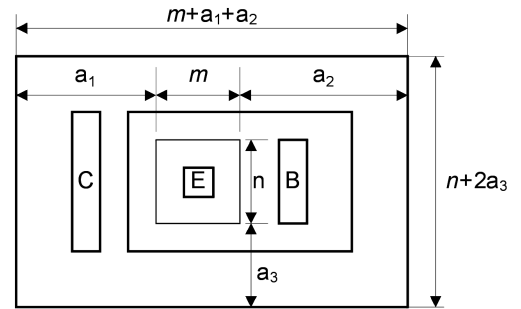


Fig. 3. Layout of $n-p-n$ transistor.

Probabilistic characteristics of parameters V_{Be} , and β weakly depend on dimensions of transistors. The mean and standard deviation of r_b depends on the width (n) and the length (m) of transistor emitters. The dimensions of the transistor are closely related to dimensions of the emitter (Fig. 3). The statistics of transistor pa-

rameters V_{Be} , β , r_b was processed for various values of n and some fixed values of m . The problem was solved on conditions that probabilistic characteristics of V_{Be} , and β as well as correlation coefficients between the all IP are independent of dimension variations and that mean values of resistance of resistors and layer resistivity with resistors are predetermined.

Means and standard deviation dependences of parameters of elements on their dimensions obtained using ESA are given in Table I. The correlation coefficients between the parameters are presented in Table II. In Table I $A_1, B_1, C_1, F_1, G_1, H_1, H_2, H_3, H_4, h, \delta$ are parameters that characterize the level of process technology and are determined from approximations of experimental curves. In Table II $i, j = 1, 2, \dots, 8; t, g = 1, 2, \dots, 10$. The width of emitters of transistors V1 and V2, V4 and V5, V6 and V7, which are indicated as n_1, n_4, n_6 , accordingly, and the width of resistors R1, R2, R4–R9 $d = d_1 = d_2 = d_4 = d_5 = d_6 = d_7 = d_8 = d_9$ were used as variables. The problem was solved under condition that all transistors have the same fixed length of emitters $m = 1.0 \mu\text{m}$.

TABLE I
Mean and standard deviations.

Parameter	Mean	Standard deviation
$\beta_1-\beta_8$	100	$100H_1$
$V_{Be1}-V_{Be8}$ [V]	0.73	$0.73H_2$
r_{b1}, r_{b2} [Ω]	$F_1m_1/n_1 + G_1/n_1$	$A_1 + B_1/m_1 + C_1/n_1$
r_{b4}, r_{b5} [Ω]	$F_1m_4/n_4 + G_1/n_4$	$A_1 + B_1/m_4 + C_1/n_4$
r_{b6}, r_{b7} [Ω]	$F_1m_6/n_6 + G_1/n_6$	$A_1 + B_1/m_6 + C_1/n_6$
r_{b3}, r_{b8} [Ω]	2000	$2000H_3$
R1, R2 [Ω]	1500	$1500(h/d_1 + \delta)$
R3, R10 [Ω]	750	$750H_4$
R4, R6 [Ω]	900	$900(h/d_4 + \delta)$
R5, R7 [Ω]	3000	$3000(h/d_5 + \delta)$
R8, R9 [Ω]	1500	$1500(h/d_8 + \delta)$

TABLE II
Correlation coefficients.

	β_j	V_{Bej}	r_{bj}	R_g
β_i	0.8	-0.6	0.8	-0.15
V_{Bei}		0.9	-0.7	0
r_{bi}			0.9	-0.2
R_t				0.95

TABLE III
Optimal dimensions of elements.

Process technology	N_1 [μm]	N_4 [μm]	N_6 [μm]	D [μm]	Y_T
0.15 μm	1.0	0.8	0.8	1.1	4646
0.25 μm	1.4	0.9	1.0	1.9	3687
0.35 μm	3.0	1.3	1.5	3.1	1940

By means of the IC model, PIP (Tables I, II) and requirements for parameters, for every concrete set of the

values of n_1, n_4, n_6, d , the Y_p was calculated by the Monte Carlo method and the S_c was estimated. Using a well known equation $Y_c = \exp(-\lambda\eta S_c)$ (λ is the mean defect density on the wafer, η is the probability that a defect makes a chip bad) the catastrophic yield was estimated, and knowing S_w the Y_T was calculated using (1). The aim of the problem was the determination of values $n_1 = N_1, n_4 = N_4, n_6 = N_6$ and $d = D$, at which Y_T is maximal. The values of N_1, N_4, N_6 and D were determined by means of optimization methods presented in [2, 3] for three levels of process technology: 0.18, 0.25 and 0.35 μm . The results for $S_w = 7800 \text{ mm}^2$ and requirements for IC parameters $|U_{OS1} \div U_{OS4}| < 2 \text{ mV}$ are presented in Table III and Fig. 4.

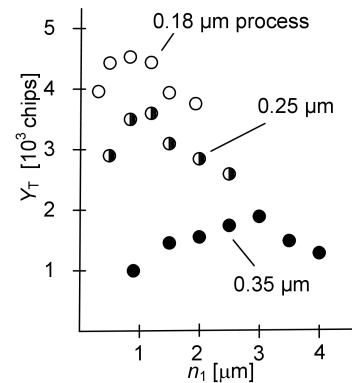


Fig. 4. The dependences of the IC yield on the width of the V1, V2 transistor emitters for various levels of the IC process technology at optimal values of n_4, n_6 and d .

4. Conclusions

The results of differential amplifiers IC yield analysis obtained using the suggested technique allow us to draw up the following conclusions, which can be important in the design of analog ICs based on the differential amplifiers:

1. The optimal values of dimensions of elements by IC yield maximum criteria depend on the level of process technology and requirements for IC parameters;
2. The optimal values of dimensions of elements, which perform the same function but are located in the different stages of the differential amplifier (e.g. V1, V2 and V6, V7), are different.

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