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Phase Noise Minimization in CMOS Voltage Controlled Oscillators

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Relaxation RC type voltage controlled oscillator is more desirable for many applications because of wide frequency generation range, small size on chip and linear voltage to frequency transfer characteristic. The limiting factor of such voltage controlled oscillator type is that it has higher phase noise in comparison with liquid crystal oscillators. We discuss how different device components, parameters and configuration influence phase noise, including transistor noise sources dependence on its geometrical parameters. The simulation results of the relaxation voltage controlled oscillator which was implemented in different 180 nm and 90 nm CMOS technologies are reported.

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1. Introduction

Voltage controlled oscillator (VCO) is one of the key components of a phase locked loop (PLL), which is used in various synchronization schemes. One such application, which is mostly concerned in this paper, is in detail described in [1].

Relaxation RC type VCO has notable advantages in comparison with LC VCO, such as wide frequency range, small size on chip which means low cost, linear voltage to frequency transfer characteristic, but it has higher phase noise. Thus phase noise minimization in relaxation VCO is very important issue.

By definition, phase noise of an oscillatory system is a measure of random deviations of its oscillation frequency from a nominal value. Deviations mentioned above are caused by various noise sources, which modulate oscillation frequency. Main contribution to noise gives active devices, in our case MOS transistors and device configuration which is described in Sect. 2. That is why it is very important to evaluate their noise and its dependence on geometry and technology. These issues are discussed in Sect. 3.

Section 4 is dedicated to presentation and discussion of relaxation VCO simulation results.

2. Relaxation VCO configuration and phase noise minimization

Figure 1 shows the schematics of a VCO. As it was already mentioned important device's parameter is size on chip. Capacitor C1 influences mostly size and phase noise of a VCO. In [2] an equation (1) is derived for a minimum achievable phase noise of an ideal relaxation voltage controlled oscillator, which evaluates only resistor's equilibrium thermal noise current given by $4kT/R$. This equation cannot calculate exact phase noise in relaxation RC VCO, but it can predict noises behavior

$$PN_{\min}(\Delta f) \approx \frac{5.9 f_0 kT}{C V_{dd}^2 (\Delta f)^2} \approx \frac{3.1 kT}{P_{\min}} \left(\frac{f_0}{\Delta f}\right)^2, \qquad (1)$$

where $P_{\min} = 0.52 f_0 V_{dd}^2 C$ is consumed power, f_0 — central frequency, C — capacitance, Δf — offset frequency, V_{dd} — supply voltage, k — the Boltzmann constant, T — temperature. The smaller capacitor value and, respectively, power consumption are, the higher the phase noise is. We need to take into account all dominant noise sources of MOS transistor and evaluate short channel effects to get more precise results.

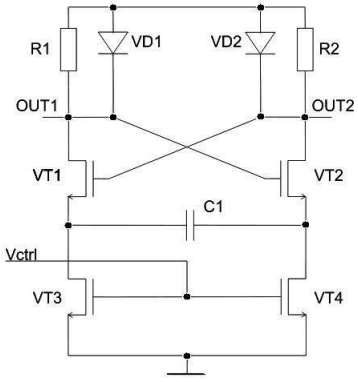

Fig. 1. Schematics of relaxation voltage controlled oscillator.

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Another well known approach of a phase noise minimization is a cross-coupling of oscillators. Due to additional coupling current switching speeds up. Oscillator spends less time in the transition between two states so the time window for noise sources to act and produce phase noise is narrower. Simulated and measured data in [3] shows that strongly coupled RC VCO inherits much better phase noise. According to [2] such method is not particularly useful because M optimally coupled oscillators improve phase noise M times, but also they consume M times more power. Equation (1) shows that the same minimum achievable phase noise improvement is possible if we simply increase power consumption of a single oscillator M times.

3. MOS transistor noise

Downscaling CMOS technology not only strongly improves RF performance of MOS devices, but also adds short channel effects (SCE). Several recent studies on a RF CMOS noise modeling [4, 5] shows that classical noise modeling approaches, e.g. BSIM v3.3 remains valid for technologies down to 90 nm if SCEs and parasitic resistances that surround the MOSFET are properly evaluated.

There are three main noise sources in MOSFET which are flicker or $1/f$ noise, drain current and gate current thermal noises.

For a flicker noise a unified $1/f$ noise model was developed. It describes measured noise both in n-channel and p-channel devices very successfully and is used in most today's noise models, e.g. BSIM v3 and v4, MOS MODEL 9 and 11.

According to [4] 0.18 μm MOS transistor drain current noise S_{Id} consists of its intrinsic thermal noise by 88%. Next highest contribution gives additional gate resistance induced drain current noise.

Contribution to overall gate current noise S_{Ig} of an intrinsic MOSFET gate current noise is only about 30%. Another 30% is due to effective gate resistance which is caused by contact resistance between silicide and polysilicon and cannot be reduced. Third 30% part of noise is also due to gate resistance, but it is layout dependent and can be reduced through careful layout optimization.

One more investigation on sub-100 nm MOSFETs [5] shows similar to previously discussed results. Gate resistance induced noise contribute almost all of gate current noise and about 15% of drain current noise in 65 nm devices. Generally S_{Id} is larger in devices with shorter gate length due to larger g_{do} output conductance at zero drain-source bias and shorter effective channel length. Gate scaling has an opposite effect on a gate current noise — it decreases due to smaller gate capacitances C_{gs} and C_{gg}.

4. Simulation results and discussion

In order to verify previously discussed phase noise minimization, Cadence software simulations with CMOS 180 nm and 90 nm BSIM v3.3 models were done. 640 MHz VCO center frequency is selected, temperature to 300 K is set and phase noise at 1 MHz offset frequency is measured to achieve the same simulation conditions.

Firstly we simulate phase noise dependence on capacitor C1 value (Fig. 2). VT1 and VT2 transistors width is set to 20 μm in order to avoid parasitic capacitance influence.

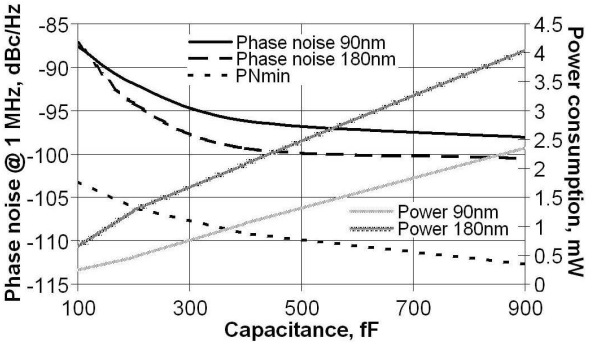

Fig. 2. Phase noise with 1 MHz offset frequency and power consumption versus capacitance.

We vary C1 value from 100 to 900 pF and measure phase noise and power consumption. Simulations show that behavior of phase noise both for 180 nm and 90 nm is similar to minimum achievable phase noise which was predicted by Eq. (1) and is shown in Fig. 2 as "PNmin". Difference between minimum achievable and simulated phase noise is called a wastefulness factor, which is caused by constant current flow through the oscillator and other noise sources which were not taken in account by (1).

Second simulation results show how phase noise and power consumption of VCO depend on transistors VT1 and VT2 widths (Fig. 3). Capacitor C1 values are 400 fF and 800 fF. Transistors widths were varied from 10 μm to 90 μm. When transistor width is smallest, phase noise has highest values. If transistor width increases, the g_{m}, current through transistor and oscillator consumed power increases as well. According to (1) and Fig. 3 higher power means lower phase noise. Its value reaches minimum at some point for each technology and capacitance. At this point other than transistor VCO elements start to limit current flowing through circuit. Further increase of transistor width and correspondingly g_{m} increases the phase noise. Figure 3 shows that consumed power and respectively phase noise of 90 nm technology with 800 fF capacitor and 180 nm technology with 400 fF capacitor are very similar.

Several simulations were performed in order to determine whether cross-coupling of oscillators improves phase noise. Firstly phase noise of a single VCO with capacitance value 400 fF, transistors dimensions $W/L = 0.18/20$ μm were simulated and showed -99.3 dBc/Hz phase noise. Then phase noise of two cross-coupled VCOs with the same parameters and 1.5 mA coupling current were simulated. Such configuration has -103 dBc/Hz

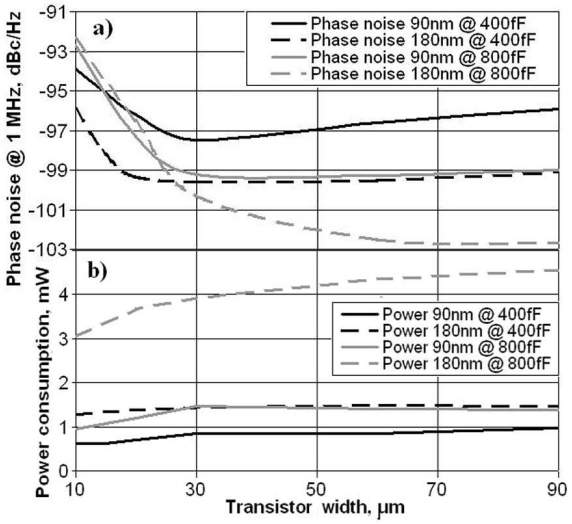

Fig. 3. (a) Phase noise with 1 MHz offset frequency and (b) power consumption versus transistor width with 400 fF and 800 fF capacitances.

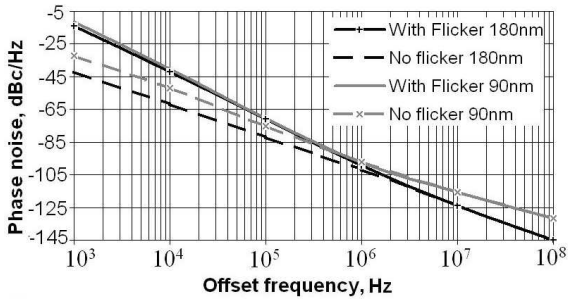

Fig. 4. Phase noise versus offset frequency for a 90 nm and 180 nm technologies, $W = 30$ μm, $C = 400$ fF.

phase noise which gives 3.7 dBc/Hz improvement over single VCO. Also phase noise of single VCO with doubled capacitance value ($C = 800$ fF) and doubled transistor width ($W/L = 0.18/40$ μm) was simulated. It has -102.1 dBc/Hz phase noise. So, VCO cross-coupling, as a technique for phase noise minimization, is practically not very useful because achieved phase noise improvement is less than 1 dBc/Hz.

In order to define flicker noise contribution to overall noise of a VCO for different technologies simulations with $1/f$ noise (Fig. 4, solid lines) and without it (Fig. 4, dashed lines) were performed.

Flicker noise increases phase noise at 1 MHz offset frequency by 2.5 dB for a 180 nm and only by 0.5 dB for 90 nm. $1/f$ noise becomes dominant for lower offset frequencies. So, in order to minimize phase noise at offset frequencies of interest thermal noise should be minimized, as it was discussed in the Sect. 3.

5. Conclusions

180 nm technology shows better phase noise performance than 90 nm thus it should be used to minimize phase noise. Thermal noise should be mostly considered in order to minimize VCO phase noise. VCO with highest capacitance value $C = 900$ fF shows minimum -98.1 and -100.5 dBc/Hz phase noise for 90 nm and 180 nm technologies, respectively. Optimal transistor widths for 180 nm and 90 nm technologies are 26 μm and 29 μm with 400 fF capacitance and 35 μm and 65 μm with 800 fF, respectively. VCO cross-coupling is not particularly suitable technique for phase noise to power ratio minimization.

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