Frequency Dependent Electrical Characteristics of Au/*n*-Si/CuPc/Au Heterojunction

Z. Ahmad, M.H. Sayyad*, Kh.S. Karimov, M. Saleem and M. Shah
Ghulam Ishaq Khan Institute of Engineering Sciences and Technology, Topi-23640, NWFP, Pakistan

(Received February 14, 2008; in final form October 19, 2009)

Electrical characteristics of the heterojunction fabricated by thermal deposition of copper phthalocyanine (CuPc) on an n-silicon substrate have been investigated. The frequency has significant effect on capacitance (C), conductance (G) and series resistance (R_s) interface states (D_{it}) of the junction. Measured capacitance and conductance were corrected for R_s. The conductance technique was used to measure the density of the interface states. This method revealed the value of the interface state density distribution for the Au/n-Si/CuPc/Au interfaces of the order of 10^{12} cm^{-2} eV^{-1}.

PACS numbers: 79.60.Jv, 73.90.+f

1. Introduction

Organic/inorganic heterojunctions have wide applications in solar cells, photodetectors, light emitting diodes, communication systems, and industry [1–5]. The generation of interface traps are one of the main reasons of instability and poor performance of these devices [6]. These defects are generated because the junction contacts have a metal/interfacial layer/semiconductor (MIS) structure instead of metal/semiconductor (MS) due to thin interfacial native oxide layer between the metal and the semiconductor [5]. The existing insulating layer converts MS structure to MIS structure. The device stores the electric charge due to the dielectric property of oxide layer, and behaves as a capacitor. When voltage is applied across the MIS structure, the series resistance, depletion layer, and interfacial insulator layer, all share applied voltage [7].

The first investigation on the MIS contacts was done in Ref. [8], the authors estimated interface state energy distribution from an analysis of barrier height. Later on [9–11] it was showed that both the interface state energy distribution and the interfacial layer thickness can be determined by I–V characteristics. Recently some authors [12–14] have studied the effect of an interface state density on series resistance from frequency dependent C–V curves. In the idealized case, the C and G plots are frequency independent. However, the presence of an interfacial layer between the contact materials and interface states at the semiconductor layers disturbs this idealized case [14–16].

This paper reports the investigation of electrical characteristics of the Au/n-Si/CuPc/Au heterojunction. The effects of frequency on series resistance of the junction have been studied, because the series resistance plays an important role for understanding of the electrical properties and performance of the devices.

2. Experimental

The Au/n-Si/CuPc/Au heterojunction was fabricated by evaporating copper phthalocyanine (Sigma Aldrich) in high vacuum on n-silicon substrate with (110) orientation. Prior to deposition, the substrate was cleaned in ultrasonic bath of acetone and dried. During thermal deposition, the substrate was kept at room temperature and the base vacuum was 5.5×10^{-3} Pa. A 30 nm thick film of CuPc was deposited using mask at a growth rate of 0.1 nm s^{-1}. The thickness was monitored by quartz crystal monitor. The active area of n-Si/CuPc junction was 125 mm^2. The ohmic contacts on CuPc and n-Si were deposited by evaporating Au. The thickness and area of the both contacts were 100 nm and 50 mm^2, respectively. All the measurements were performed at room temperature. Functional testing on the heterojunction was done using a KARL SUSS PM5 probe station.

3. Results and discussion

Usually in the laboratory environment the inorganic semiconductors surfaces are covered with layers of native oxides. The native oxide layers grow on chemically

* corresponding author; e-mail:
sayyad@giki.edu.pk, hsayyad62@hotmail.com

prepared semiconductor surfaces even when they are exposed to clean room air [13]. So there is possibly an insulating oxide layer between CuPc and the n-Si substrate. The interface oxide layers grow during surface preparation, metal evaporation, and post-deposition thermal annealing [16, 17]. When MS contact with inter-facial layer is considered, it is assumed that the current through the interface is due to thermionic emission and can be expressed as [18]:

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right], \tag{1}$$

where I_0 is the saturation current and can be given as

$$I_0 = AA^*T^2 \exp\left(\frac{q\phi_{b0}}{kT}\right), \tag{2}$$

where V is the bias voltage, A is the effective diode area, A^* is the effective Richardson constant (112 ± 6 A cm^{-2}K^{-2} for n-type Si), ϕ_{b0} is the zero-bias barrier height and n is the ideality factor. Value of ideality factor n can be expressed as

$$n = \frac{q}{kT}\left(\frac{\mathrm{d}V}{\mathrm{d}\ln I}\right). \tag{3}$$

The frequency dependent capacitance and the conductance of the device can be used to calculate interface properties. Various techniques have been used to achieve this. One of the techniques is conductance technique, which determines the point-to-point density of states throughout the depletion region of such devices [19]. The conductance technique determines the surface parameters with more accuracy than capacitance technique [20] because the conductance comes only from the interface states [19]. The conductance losses are the base of conductance technique resulting from the exchange of majority carriers between the interface states, when a small AC signal is applied to the devices [21]. In depletion region the DC biased Fermi level starts to oscillate about the mean position by applying AC signal [22]. So it is assumed that there may be a capacitance due to interface states in excess to depletion layer capacitance, which depends upon the relaxation time of the interface states and the frequency of the AC signal.

Capacitance as a function of voltage for Au/n-Si/CuPc/Au heterostructure is shown in Fig. 1. The three distinct regions of accumulation, depletion, and inversion can be seen. The value of capacitance increases with the decrease in frequency. This may be due to the time dependent response of interface states [22].

Figures 2 and 3 show the measured capacitance (C) and measured conductance (G/ω) of Au/n-Si/CuPc/Au heterostructure in depletion region as a function of the frequency at different bias voltages. At higher frequencies capacitance remains almost constant, while at the lower frequencies capacitance and conductance change. This means that at higher frequencies, the interface states cannot follow the AC signal [23] and consequently cannot contribute much to the capacitance. It indicates that the interface states are responsible for the observed frequency dispersion in C and G/ω curves.

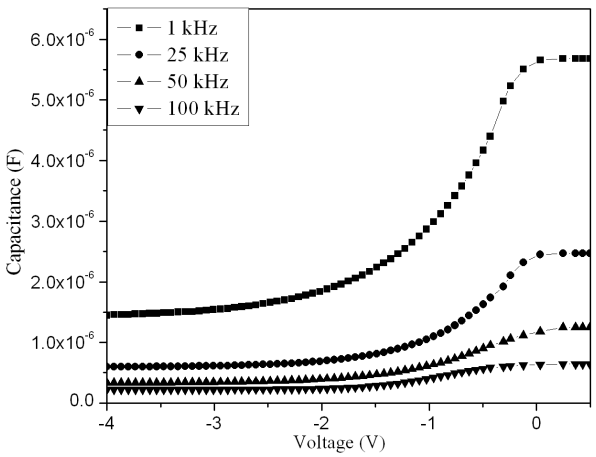

Fig. 1. C–V curves of the Au/n-Si/CuPc/Au heterostructure at different frequency.

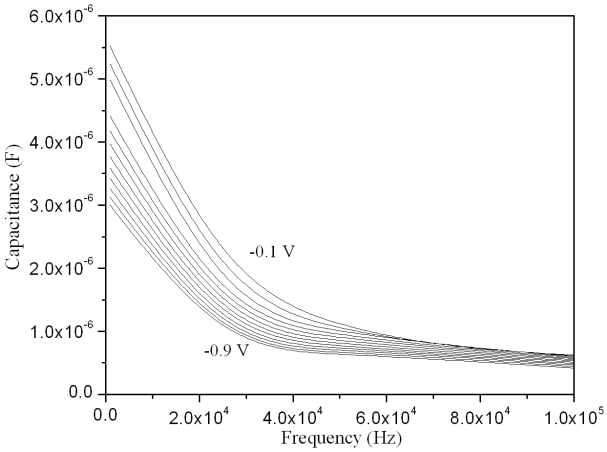

Fig. 2. C–f characteristics of Au/n-Si/CuPc/Au structure at different biases.

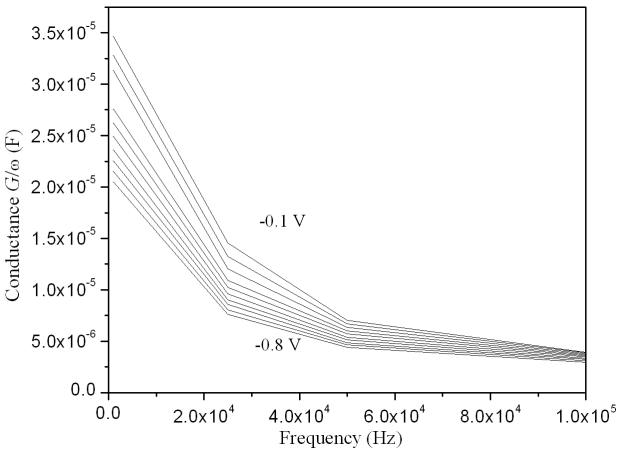

Fig. 3. G/ω–f characteristics of Au/n-Si/CuPc/Au structure at different biases.

Actually CuPc is a molecular semiconductor in which electronic states are localized unlike to conventional semiconductor such as Si, Ge and GaAs etc., where the states are delocalized. In organic semiconductors the hopping lengths of electrons are much smaller than the free path lengths of electrons in conventional semiconductor. Therefore, conductivity of organic semiconductors is sensitive much to frequency of applied AC signals. The real series resistance of the structure can be determined from the measured capacitance and conductance in strong accumulation region [12, 21]. The series resistance, when the MIS structure is in strong accumulation region, can be represented as [21]:

$$R_{\mathrm{s}} = \frac{G_{\mathrm{acc}}}{G_{\mathrm{acc}}^2 + \omega^2 C_{\mathrm{acc}}^2}\,, \tag{4}$$

where G_{acc} and C_{acc} are measured conductance and capacitance in strong accumulation region, respectively. The capacitance of insulator oxide layer (C_{ox}) is related to series resistance given by [21]:

$$C_{\mathrm{acc}} = \frac{C_{\mathrm{ox}}}{1 + \omega^2 R_{\mathrm{s}}^2 C_{\mathrm{ox}}^2}\,. \tag{5}$$

From Eqs. (4) and (5), C_{ox} can be written as

$$C_{\mathrm{ox}} = C_{\mathrm{acc}} \left[1 + \left(\frac{G_{\mathrm{acc}}}{\omega C_{\mathrm{acc}}}\right)^2\right]. \tag{6}$$

The series resistance vs. frequency for Au/n-Si/CuPc/Au is plotted in Fig. 4. The corrected capacitance (C_{c}) and corrected equivalent parallel conductance (G_{c}) for series resistance are obtained as a function of angular frequency from the measured capacitance and conductance by [21]:

$$C_{\mathrm{c}} = \frac{\left(G_{\mathrm{m}}^2 + \omega^2 C_{\mathrm{m}}^2\right) C_{\mathrm{m}}}{a^2 + \omega^2 C_{\mathrm{m}}^2} \tag{7}$$

and

$$G_{\mathrm{c}} = \frac{\left(G_{\mathrm{m}}^2 + \omega^2 C_{\mathrm{m}}^2\right) a}{a^2 + \omega^2 C_{\mathrm{m}}^2}\,, \tag{8}$$

where

$$a = G_{\mathrm{m}} - \left(G_{\mathrm{m}}^2 + \omega^2 C_{\mathrm{m}}^2\right) R_{\mathrm{s}}\,.$$

As discussed above, in the depletion and accumulation region, measured C and G/ω are highly dependent on frequency. The measured capacitance and conductance were corrected for the effect of series resistance using Eqs. (7) and (8) as shown in Figs. 5 and 6, respectively.

A reliable and fast way to determine the density of interface states (D_{it}) is the Hill–Coleman method [24], which is confirmed by Konofaos [25] and Dakhel [26]. D_{it} can be obtained according to this method by using the relation

$$D_{\mathrm{it}} = \frac{2}{qA} \frac{G_{\mathrm{m,max}}/\omega}{\left[\left(G_{\mathrm{m,max}}/\omega C_{\mathrm{ox}}\right)^2 + \left(1 - C_{\mathrm{m}}/C_{\mathrm{ox}}\right)^2\right]}\,, \tag{9}$$

where q, A and ω are elementary electrical charge, area of the junction, and the angular frequency, respectively. The calculated values of D_{it} are of the order of 10^{12} eV^{-1} cm^{-2} that is not high enough to pin the Fermi level of the n-Si substrate [25].

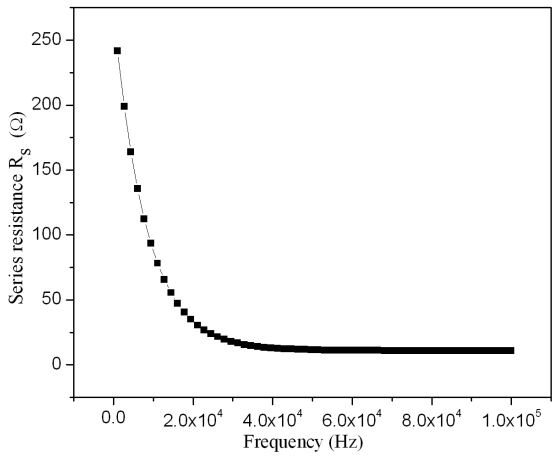

Fig. 4. Series resistance vs. frequency plot of Au/n-Si/CuPc/Au heterostructure.

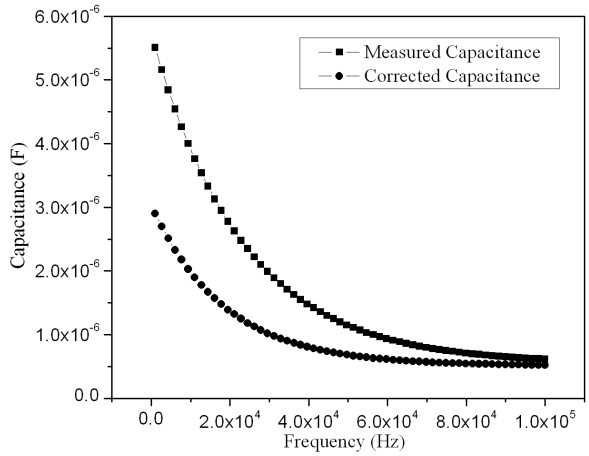

Fig. 5. The frequency dependent plot of corrected capacitance.

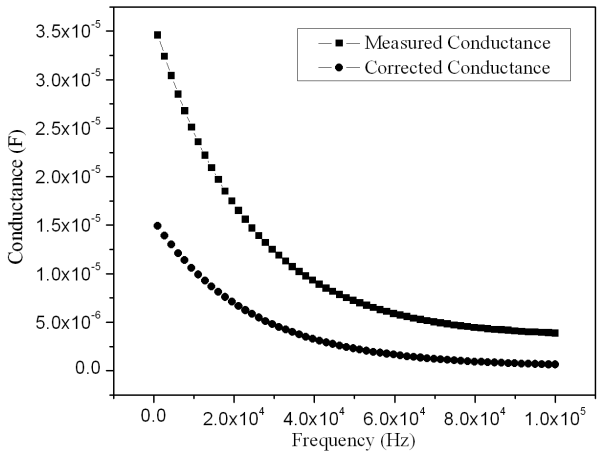

Fig. 6. The frequency dependent plot of corrected conductance.

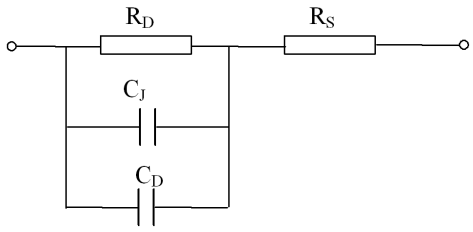

Fig. 7. Equivalent circuit diagram of Au/n-Si/CuPc/Au heterostructure.

TABLE

Values of C_{J}, C_{D}, and C_{total} at different frequencies.

Frequency [kHz]	Junction capacitance (C_{J})	Diffusion capacitance (C_{D})	Total capacitance (C_{total})
1	1.4×10^{-6}	4.4×10^{-6}	5.8×10^{-6}
25	5.9×10^{-7}	1.8×10^{-6}	2.4×10^{-6}
50	3.6×10^{-7}	8.4×10^{-7}	1.2×10^{-6}
100	2.2×10^{-7}	4.2×10^{-7}	6.4×10^{-7}

The equivalent circuit of the device is shown in Fig. 7, where R_{D}, R_{s}, C_{J}, C_{D} are the diffusion resistance, series resistance, junction capacitance, and diffusion capacitance, respectively. If the frequency approaches to infinity, then the impedance (Z) is reduced to R_{s}. If the frequency approaches to zero, then the Z is the sum of R_{s} and R_{D}. The total capacitance of the junction is given by $C_{\mathrm{total}} = C_{\mathrm{J}} + C_{\mathrm{D}}$. The values of C_{J}, C_{D} and C_{total} at different frequencies are shown in Table.

4. Conclusion

It is observed that both the capacitance and conductance are very sensitive to frequency especially at relatively low frequencies. The values of series resistance, capacitance, and conductance decrease with the increase in frequency. The C–V characteristics show that the device behaves like MIS devices. It is found that the value of interface trap density (10^{12} eV^{-1} cm^{-2}) is not high enough to pin the Fermi level of n-Si substrate. The electrical properties of the heterostructure can be controlled by interface states, which are responsible for trapping of charges and result in non-ideal behavior of C–V characterization.

Acknowledgments

The authors would like to thank the Ghulam Ishaq Khan Institute of Engineering Sciences and Technology for support by providing the necessary research facilities.

References

[1] S. Riad, *Thin Solid Films* **370**, 253 (2000).

[2] S.A. Moiz, M.M. Ahmed, Kh.S. Karimov, *Jpn. J. Appl. Phys.* **44**, 1199 (2005).

[3] S. Darwish, *Egypt J. Solids* **26**, 55 (2003).

[4] M.M. Ahmed, Kh.S. Karimov, S.A. Moiz, *IEEE Trans. EDS* **51**, 121 (2004).

[5] M.E. Aydin, F. Yakuphanoglu, Jae-Hoon Eom, Do--Hoon Hwang, *Physica B* **387**, 239 (2007).

[6] P. Hanselaer, W.H. Laflere, R.L. Van Meirhaeghe, F. Cardon, *Appl. Phys.* **56**, 2309 (1984).

[7] I. Yucedag, S. Altindal, A. Tataroglu, *Microelectr. Eng.* **84**, 180 (2007).

[8] A.M. Cowley, S.M. Sze, *J. Appl. Phys.* **36**, 3212 (1965).

[9] H.C. Card, R.H. Rhoderick, *J. Appl. Phys.* **4**, 1589 (1971).

[10] H. Tseng, C. Wu, *Solid-State Electron.* **30**, 383 (1987).

[11] Z.S. Horvath, *J. Appl. Phys.* **63**, 976 (1988).

[12] S. Karadeniz, N. Tugluoglu, T. Serin, *Appl. Surf. Sci.* **233**, 5 (2004).

[13] S. Karadeniz, N. Tugluoglu, T. Serin, N. Serin, *Appl. Surf. Sci.* **246**, 30 (2005).

[14] A. Singh, *Solid-State Electron.* **28**, 233 (1985).

[15] E.H. Nicollian, A. Goetzberger, *Bell. Syst. Technol. J.* **46**, 1055 (1967).

[16] E.H. Rhoderick, R.H. Williams, *Metal–Semiconductor Contacts*, 2nd ed., Clarendon Press, Oxford 1988.

[17] P. Cova, A. Singh, A. Medina, R.A. Masut, *Solid--State Electron.* **42**, 477 (1998).

[18] E.H. Rhoderick, *Metal–Semiconductor Contacts*, Oxford University Press, Oxford 1978.

[19] S. Logothetidis, *J. Appl. Phys.* **82**, 5017 (1997).

[20] E.H. Nicillian, A. Goetzberger, *Appl. Phys. Lett.* **7**, 216 (1965).

[21] E.H. Nicollian, J.R. Brews, *MOS Physics and Technology*, Wiley, New York 1982.

[22] S. Karadeniz, A. Birkan Selcuk, N. Tugluoglu, S. Bilge Ocak, *Nucl. Instrum. Methods Phys. Res. B* **259**, 889 (2007).

[23] J. Fernandez, P. Godignon, S. Berberich, J. Rebollo, G. Brezenanu, J. Millan, *Solid-State Electron.* **39**, 1359 (996).

[24] W.A. Hill, C.C. Coleman, *Solid State Electron.* **23**, 987 (1980).

[25] N. Konofaos, *Microelectr. J.* **35**, 421 (2004).

[26] A.A. Dakhel, *Thin Solid Films* **496**, 353 (2006).