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Nanoscale Pattern Definition by Edge Oxidation of Silicon under the Si_3N_4 mask — PaDEOx

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Well-controlled method of Si nanopattern definition — pattern definition by edge oxidation have been presented. The technique is suitable for fabrication of narrow paths of width ranged from several tens of nm to several l'm by means of photolithography equipment working with l'm-scale design rules. Process details influencing a shape of the Si pattern have been discussed. SEM examinations have been presented.

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1. Introduction

The dimensions of modern microdevices become smaller and smaller. Thus, there is a huge demand and interest in introducing new technologies and tools in microfabrication. As a rule it is associated with the appreciable outlay for hardware upgrade. Sometimes, however, a creative approach to the manufacturing issues like in the case of spacers [1, 2], nanoribbons [3] or so-called lateral pattern definition technique [4, 5] can make downsizing less expensive.

In this work, we investigate the possibility of submicron patterning of silicon by edge oxidation under silicon nitride mask (pattern definition by edge oxidation, PaDEOx).

2. Experimental

The fabrication sequence of a Si nanopath is presented in Fig. 1. ⟨100⟩ oriented silicon wafers of any desired conductivity were wet oxidized to an oxide thickness required for a final structure. Subsequently, the SiO_2 layer was covered with Si_3N_4 obtained by low pressure chemical vapor deposition (LPCVD); the thickness of the nitride layer varied from 40 to 130 nm for the oxide thickness below 40 nm and *ca.* 1 μm thick film, respectively. The SiO_2/Si_3N_4 sandwich was patterned using conventional photolithography, dry etching of Si_3N_4 and wet etching of SiO_2 (Fig. 1A). Then, the silicon exposed through the nitride masking layer was oxidized to an oxide thickness similar to that obtained at the first oxidation cycle. Since the oxidizing species diffuse laterally, the oxidation occurs also under the edge of nitride film causing so-called "bird's beak" known from the LOCOS (local oxidation) process (Fig. 1B). The oxide thickness in the edge areas was higher than that on the ⟨100⟩ wafer surface. Afterwards, the Si_3N_4 masking layer was etched away by selective wet etching step (Fig. 1C), while the oxide was wet etched till it disappeared from the flat wafer surface but remained locally along the edge of the former sandwich areas (Fig. 1D). In this way, the silicon surface was covered with the narrow SiO_2 stripes, which acted as a mask in subsequent dry etching of Si (Fig. 1E) using so-called Bosch process (a technique consisting of alternating etch and deposition cycles to produce high aspect-ratio features; SF_6 and C_4F_8 were used as an etchant gas and polymer deposition gas, respectively). Finally, the oxide stripes were removed by wet etching in hydrofluoric acid.

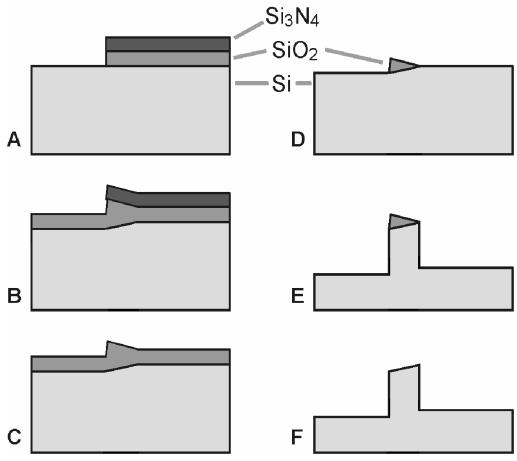

Fig. 1. The cross-sections corresponding to subsequent fabrication steps of silicon nanopath.

3. Results and discussion

Figure 2 shows a cross-section of a typical silicon nanoscale path obtained using PaDEOx method. Such a structure is created as a closed loop around a pattern, which has been defined earlier by other method; in order to obtain a long narrow length of the Si path an additional photolithography step is required. It may seem that the height of the feature depends on the depth (time) of silicon dry etching, while its width is determined by the

width of the masking oxide stripe. However, the feature height is only dependent on vertical etching progress and the width and shape are influenced by numerous factors including selectivity during wet etching, oxidation conditions, oxides thickness ratio, silicon nitride thickness, and dry etching conditions.

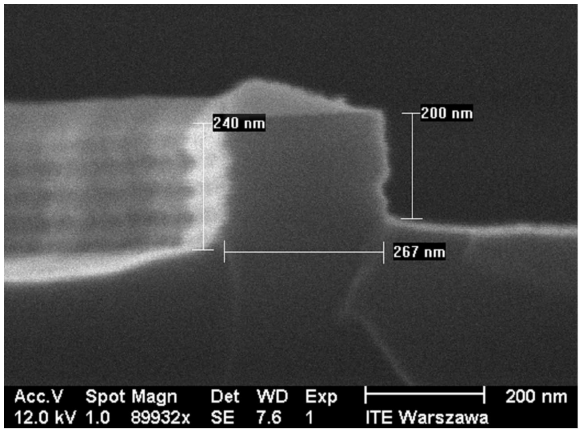

Fig. 2. The cross-section of a typical silicon nanopath obtained by PaDEOx method.

The SiO_2 etching selectivity over Si_3N_4 in a typical buffered HF solution and hot (173 ℃) H_3PO_4 was found to be about 40:1 and 1:15, respectively. The process carried out using hydrofluoric acid has also a high selectivity over Si, but carried out in ortophosphorous acid does not lead to silicon etching at all. Etching of the oxide obtained in the second cycle is a crucial step in the PaDEOx method. In order to etch the oxide in a reproducible manner the thickness of the both oxide layers — below the Si_3N_4 and around the SiO_2/Si_3N_4 sandwich area — should be similar. However, the thickness may range from several nanometers to several μm and it is only limited by the oxidation conditions. Figure 3 illustrates the relationship between the silicon nanofeature width and the thickness of SiO_2 layer obtained along the edge of the nitride mask during second oxidation at 900 ℃ and 1000 ℃. The oxidation was performed until the oxide film became thicker than that obtained in the previous oxidation cycle — the difference in thickness of both oxides complied the SiO_2 loss expected during the nitride etching due to the selectivity limitations. The lateral oxidation rate in the "bird's beak" region in relation to the vertical one was found to be higher at 900 ℃ than at 1000 ℃. Such a result was expected since the difference in oxidation rates of various silicon crystal planes is more pronounced at lower temperatures. In all the performed experiments the broadening of the lateral oxidation region on the corners was observed to be larger than along the straight edges (perpendicular or parallel to the wafer flats) of the nitride mask.

The thickness of the Si_3N_4 oxidation mask layer was 130 nm in the case of 850 nm thick oxide. In all other samples the nitride film was *ca.* twice thinner (64 nm).

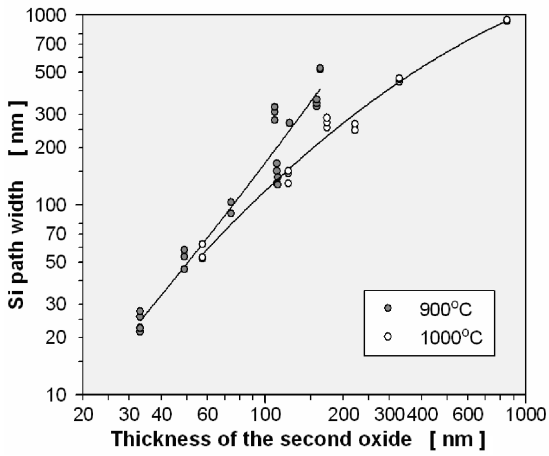

Fig. 3. Effect of the SiO_2 thickness (second oxidation) on the silicon nanopath final width.

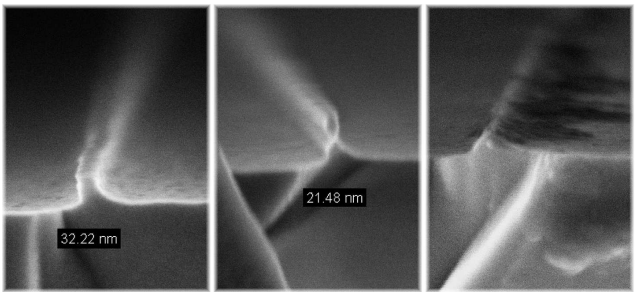

Fig. 4. The profile of silicon nanopath obtained using Bosch process for 3, 6, and 9 s.

It appeared that the nitride thickness has a minor importance in PaDEOx method. Nevertheless, it is worth noting that the lateral silicon oxidation under the mask edge goes deeper when the nitride layer is thinner — the wider the oxide masking stripe, the wider the width of a final silicon feature.

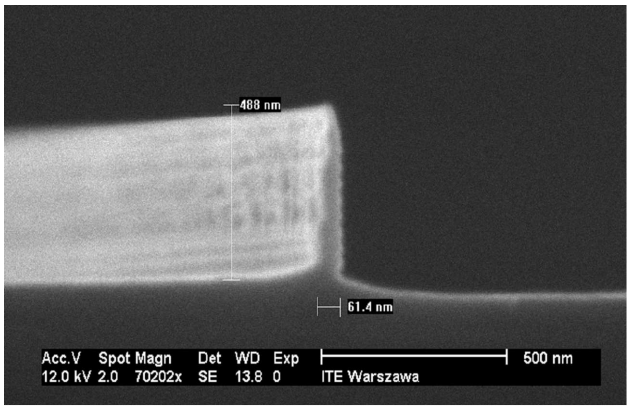

Fig. 5. High aspect ratio silicon nanopath obtained by PaDeOx method.

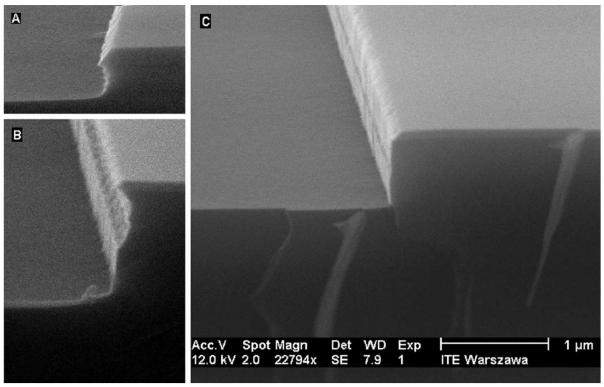

Fig. 6. Cross-sections of the nanofeature obtained using various C_4F_8 and SF_6 flows during plasma etching of Si: (A) 60/170, (B) 54/150, and (C) 60/150 sccm/min.

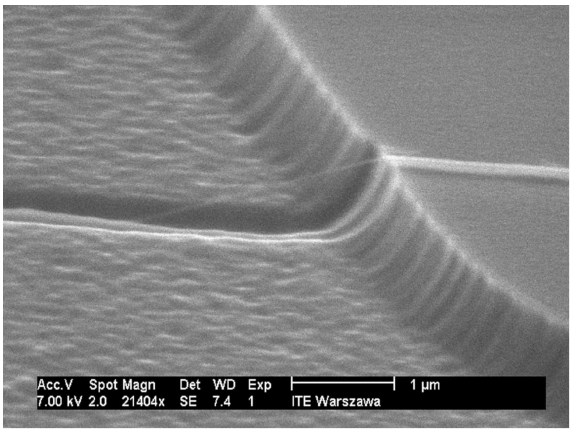

Fig. 7. The narrow silicon feature obtained by PaDeOx method and released using plasma etching.

Both the shape and dimension of the silicon nanofeature are also strongly affected by the conditions of Si dry etching. As was mentioned earlier, silicon was etched by applying series of alternating etching and deposition steps. Typically, 1 s polymerization and 2 s etching steps were used. Then the sidewalls were scalloped, which can be easily seen in Fig. 2. The process selectivity over the SiO_2 was found to be about 19:1. Thus, the oxide mask disappeared systematically during silicon etching. In Fig. 4 the profile of silicon feature after 3, 6, and 9 s process runs is presented. It is evident that the feature width decreases with etching time and that the oxide mask has been completely eroded after plasma exposure time of 10 s.

It is possible to obtain high aspect ratio features using the investigated PaDeOx method. In Fig. 5 an example of a nanostructure, whose height to width ratio is about 8, is presented. It can be seen that the sidewalls converge toward the feature top. In order to make the sidewalls more vertical and smooth the etching conditions were optimized (see Fig. 6).

Silicon nanofeature fabricated by the PaDEOx method can be underetched using isotropic dry etching of silicon, which is preceded by the passivation of vertical sidewalls with fluorocarbon polymer (see Fig. 7). The nanowire becomes separated from the substrate after dry release step and it can be a part of a sensor with the large active area or transistor with a four-sided gate surrounding the wire channel region.

4. Conclusions

The current work demonstrates capabilities of PaDEOx method, in particular the dimensions and shapes of silicon features being fabricated. The described method might be considered as an alternative to the technologies based on the expensive nanolithography processes. A FinFET transistor with a 200 nm silicon fin width [6] has already been fabricated at the ITE facility although theoretically the tools allow us manufacturing structures with 3 μm design rules. The presented method used to fabricate FinFET transistors can potentially be extended to a range of other devices e.g. sensors for biologically active molecules, or molds that allow transfer of nanoscale pattern into a cast polymer film.

Acknowledgments

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