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TEM Characterization of Polysilicon and Silicide Fin Fabrication Processes of FinFETs

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The transmission electron microscopy characterization of various silicon and silicide fin structures intended for application in FinFET devices has been performed. The results showed that transmission electron microscopy is a very useful tool for optimization of manufacturing processes of fin nanostructures in FinFETs.

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1. Introduction

In recent years the development of the electronic technology led to design of new device constructions, which allow avoiding of limitations of the conventional planar MOS technology.

An improve of MOSFET performance can be achieved by the channel or contact engineering. So called FinFET is a semiconductor device, which enables such better device performance [1]. The current flow occurs there along very thin polysilicon/silicon nanowires with a very high aspect ratio of their height to their width. When silicon in nanowires connecting the channel and the source/drain regions are replaced by metal silicide, the electrical parameters of FinFETs can be improved. Especially, the device current demonstrates higher sensitivity to the applied gate bias. Silicide nanowires also show the high reliability and a very low resistance, which is lower than that of polysilicon/silicon nanowires. The most important feature of the FinFET construction that should be checked after manufacturing is the size of nanowires, especially the accurate values of their width and height.

The aim of this paper is to demonstrate the topics where transmission electron microscopy (TEM) observations of the fabricated polysilicon/silicon and silicided polysilicon/platinum fin nanostructures can be applied for the process and design optimization.

2. Experimental

Various kinds of silicon fin structures were fabricated at Microelectronics Laboratory of the Université catholique de Louvain (UCL) by the electron beam (e-beam) lithography and subsequent plasma etching [2]. Fin structures prepared for TEM characterization of the silicidation processes in FinFETs were arranged in several squares, each 87×87 μm in size, which formed together a semiconductor test structure, designed in UCL. Each square consisted of several fin structures of different widths (30–100 nm). The length of each fin was equal to the length of square side. Fins were prepared as single bars with different width and as groups of four bars with the width equal for each group. Silicided fin structures were formed by annealing of 68 nm high silicon nanowires covered with 35 nm thick platinum layer at 400 ℃ for 2 min in rapid thermal annealing (RTA) process [2]. Cross-sectional TEM specimens were studied in the JEM-200CX transmission electron microscope operating at 200 kV.

3. Results and discussion

Two kinds of polysilicon fin structures have been characterized. The schemes of these structures are presented in Fig. 1a and 2a. The structures of the first type were rectangle shaped bars of 60 nm height and of different widths (Fig. 1a), embedded in silicon dioxide and covered with additional polysilicon layer. The second type ones were similar but with higher bars (160 nm high), surrounded on sides by approximately 20 nm thick Si_3N_4 spacers (Fig. 2a).

TEM cross-sections of the polysilicon fin structures of the first type, whose scheme is presented in Fig. 1a, are shown in Fig 1b–e. The TEM images show three single

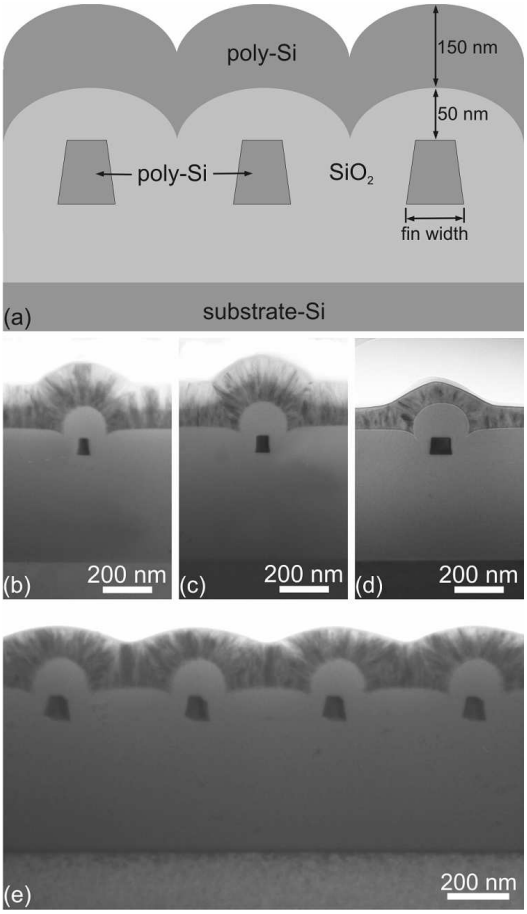

Fig. 1. Fin structures with polysilicon fins: (a) scheme of several fins (not in scale) with marked width of the nanowire and with values of designed thicknesses of poly-Si and SiO_2 layers. (b)–(e) Cross-sectional TEM images of fin structure for cases of designed width: (b) 30 nm, (c) 50 nm, and (d) 70 nm. (e) Group of four fin structures of designed fin width 50 nm.

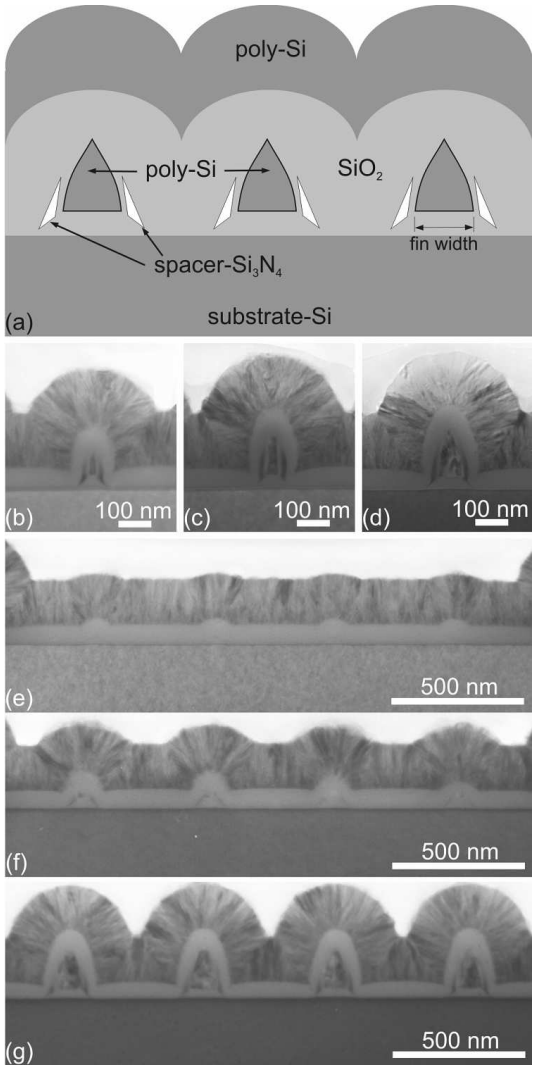

Fig. 2. Fin structures with polysilicon fins and with Si_3N_4 spacers: (a) scheme of several fins (not in scale). (b)–(g) TEM images of fin structure cross-sections for cases of designed width: (b) 50 nm, (c) 70 nm, and (d) 100 nm. Groups of four fin structures of designed widths: (e) 30 nm (as revealed, with nanowires not grown at all), (f) 50 nm, and (g) 100 nm.

polysilicon wires of designed width of 30, 50 and 70 nm and a group of 50 nm wide fin nanowires. Measurements performed on TEM images revealed that in the case of this type of fin structures, the manufactured widths of the polysilicon wires were only slightly smaller than the designed ones.

TEM cross-sections of the fin structures of the second type (with nitride spacers), whose scheme is presented in Fig. 2a, are shown in Fig. 2b–g. In this case the fin structures considerably differ from the designed ones. Namely, the manufactured widths revealed in TEM images were much smaller than the designed widths and the silicon fin shapes visible in Fig. 2 were different from the designed shapes.

As it is visible e.g. in Fig. 2e, the nanowires of the smallest widths (30 and 40 nm) have not been grown at all. It means that optimization of the structure design or of the fabrication processes is necessary, and TEM characterization appears to be very useful for that aim.

Because designed distance between nanowire centers was the same regardless the nanowire width (as seen in Fig. 2e–g), therefore the shape of polysilicon layer on the top of the structure was less or more undulated, respectively for smaller or larger fin widths.

Figure 3 shows silicon nanowires (with 100 nm width) after different silicidation processes. Silicon fin structures were covered with platinum, then subjected to annealing processes.

The TEM studies allow for determining the silicide phases that have been formed in this case. The final platinum silicide phase formed during silicidation is usually orthorhombic PtSi phase [3]. It was proved that this phase is formed in the RTA process between 300

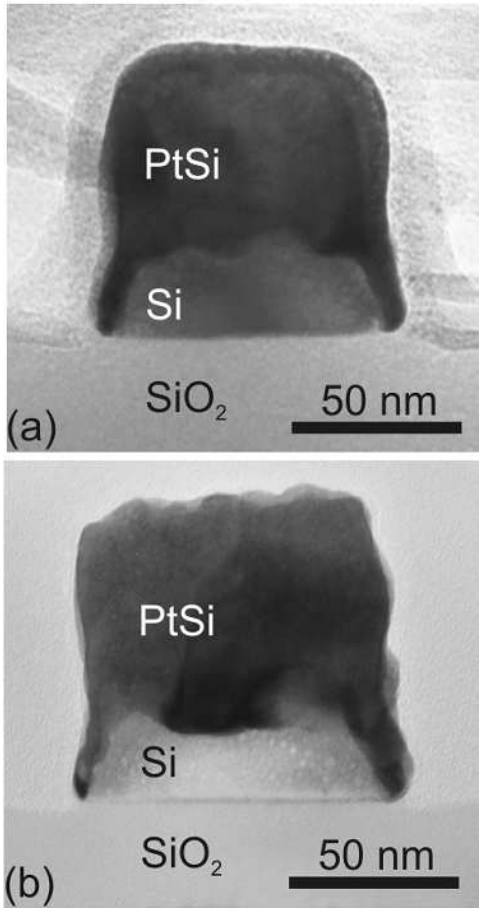

Fig. 3. (a)–(b) TEM images of cross-sections of examples of the platinum silicidation (by RTA at 400 °C for 2 min) of single silicon fin structures (with fin width equal to 100 nm).

and 500 °C for 2 min [4], which is compatible with annealing conditions used for fabrication of the structures characterized in this paper (RTA process at 400 °C for 2 min). Therefore, it can be stated that PtSi phase has been formed after platinum silicidation.

TEM cross-section images presented in Fig 3a,b illustrate the case when the silicidation process was not completed after the applied annealing conditions, because the platinum amount was insufficient to convert the whole 68 nm high silicon nanowire into PtSi. The platinum has fully reacted, while a part of the unreacted silicon is still visible. Simultaneously, negligible differences between both images of fins, shown in Fig 3a,b, prove that the silicidation process was stable and reproducible.

In order to obtain fully silicided nanowires the thickness of deposited platinum layer before annealing was increased from 35 to 50 nm, while the annealing conditions were unchanged [2].

4. Conclusions

The observations by means of the transmission electron microscopy of the structure of various polysilicon or silicided fin structures intended for the application in FinFET devices has been presented. These observations allowed for the characterization of nanostructure sizes and shapes and of their compliance with the designed ones and showed the partial completion and reproducibility of silicidation process. These results showed that generally the applied fabrication methods of fin structures were proper and that TEM can be very useful during detailed optimization of the manufacturing processes.

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