Proceedings of the XXXVIII International School and Conference on the Physics of Semiconductors "Jaszowiec" 2009

ZnO by ALD — Advantages of the Material Grown at Low Temperature

E. Guziewicz[a,*], M. Godlewski[a,b], T.A. Krajewski[a], Ł. Wachnicki[a], G. Łuka[a], W. Paszkowicz[a], J.Z. Domagała[a], E. Przeździecka[a], E. Łusakowska[a] and B.S. Witkowski[a]

[a]Institute of Physics, Polish Academy of Sciences, al. Lotników 32/46, 02-668 Warsaw, Poland

[b]Dept. of Mathematics and Natural Sciences, College of Science

Cardinal S. Wyszyński University, Warsaw, Poland

The 3D-architecture is a prospective way in miniaturization of electronic devices. However, this approach can be realized only if metal paths are placed not only at the top, but also beneath the electronic parts, which imposes drastic temperature limitations for the electronic device processing. Therefore last years a lot of investigations are focused on materials which can be grown at low temperature with electrical parameters appropriate for electronic applications. Zinc oxide grown by the atomic layer deposition method is one of the materials of choice. We obtained ZnO–ALD films at growth temperature range between 100 °C and 200 °C, and with controllable electrical parameters. Free carrier concentration was found to scale with deposition temperature, so it is possible to grow ZnO films with desired conductivity without any intentional doping. We used correlation of electrical and optical parameters to optimize the deposition process. Zinc oxide layers obtained in that way have free carrier concentration as low as 10^{16} cm^{-3} and high mobility (10–50 cm^2/(V s)), which satisfies requirements for a material used in three-dimensional memories.

PACS numbers: 73.61.Ga, 78.66.Hf, 72.80.Ey

1. Introduction

Since the invention of the integrated circuit in 1958, the number of transistors which can be placed inexpensively on one integrated circuit was doubled every second year. This long-term trend was formulated by Moore in 1965 [1] and was continued for almost fifty years. Several features of digital technology were improved exponentially according to the Moore law, like speed, cost, storage capacity, and also a size of electronic components. However, the exponential growth cannot be continued forever. The fundamental barrier of miniaturization will appear when we approach the size of atoms that was expected in the next 10 or 20 years. Before reaching this limit, last decade miniaturization accountered another problem which was a leakage current that appears in a metal–oxide–semiconductor field effect transistor (MOSFET) gate dielectric because of tunneling through a very thin gate. In order to overcome this problem, in 2007 Intel introduced hafnium dioxide [2] that replaced SiO_2 commonly used before as oxide in MOSFET. The HfO_2 dielectric constant is much higher than that of SiO_2 and therefore a thicker gate dielectric can be made for the required capacitance density [3]. Using this approach Intel was able to achieve the 45 nm technology node. Probably it will be possible to scale the same architecture to 32 nm or even to 22 nm node, but for further scaling a new concept must be introduced.

One of the new concept of miniaturization is to replace two-dimensional architecture of the present integrated circuit by three-dimensional one. This approach is intensively studied now mainly for a non-volatile memories (NVM) application. At present, the architecture of NVM is almost exclusively based on a concept of floating-gate devices, similar to that which is used in MOSFET. One of the most attractive 3D architecture is a cross-bar memory with vertically stacked memory cells [4]. In a cross-bar memory two arrays of electrodes placed perpendicular one to another are connected by a bit-storage element and a diode. The storage element can be switched between two states, "0" and "1". Provided that the diode has an appropriate I_{on}/I_{off} ratio, when applying a voltage between two crossing electrodes current will only flow through the desired node that will be read or written. This architecture will considerably improve capacitance density, because the cell area is reduced to $4F^2/n$, where F is a node standard (e.g. 45 nm) and n is a number of stacks. However, a vertically stacked architecture imposes serious materials restrictions, because metal paths here are placed not only at the top of the diode, but also below. This so-called the "back of the line" (BEOL) 3D architecture [2] requires low processing temperature which is not accessible inside silicon technology that requires temperature even at the level of 1000 °C for deposition and activate dopants [5]. In case of the 3D archi-

* corresponding author; e-mail: guzel@ifpan.edu.pl

tecture, temperature restrictions are at the level of 350 ℃ when Al is used as a metal line and 150 ℃ in case when an organic material is used as a storage element or a part of the diode. Therefore last years we observed increased interest in materials which can be successfully grown at low temperature showing electrical parameters appropriate for Schottky or p–n junctions.

Zinc oxide is regarded as a material of choice, because it can be effectively grown at low temperature limits [6–9]. ZnO is one of the most intensively investigated materials last years, because of prospective applications in light emitters, solar cells, gas sensors, piezoelectric transducers and acoustic wave devices. Recently it is also studied as a material for novel electronic devices that require low or extremely low processing temperature [10–12].

In this paper we report on structural, optical and electrical properties of zinc oxide grown by the atomic layer deposition (ALD) technique at temperature below 300 ℃. We show that physical properties of ZnO–ALD thin films make this material prospective for novel application in three-dimensional electronics.

2. Experimental conditions

For ZnO growth we used ALD which is a variant of chemical vapor deposition (CVD). The main characteristic feature of the ALD process is a sequential deposition procedure. ALD is based on surface chemical reaction between two reagents (here called "precursors") that are alternatively introduced into a growth chamber. The pulses of precursors are interrupted by purging with an inert gas, usually nitrogen. Therefore chemical reactions inside the chamber volume are effectively avoided and precursors meet and react only at the surface of the growing film. ALD is considered as one deposition method with the greatest potential for producing flat, conformal and uniform films with reproducible thickness, low stress and low defect density. This method has been applied by Intel for hafnium dioxide deposition for the 45 nm technology node, because ALD enables obtaining dense and uniform films which maintain a high dielectric constant of the bulk material.

For ZnO deposition we used diethylzinc (DEZn) as a zinc precursor and deionized water as an oxygen precursor which are commonly used for ZnO growth by ALD and CVD methods. Zinc oxide is created here as a result of a chemical reaction that takes place at the surface

$$\mathrm{Zn(C_2H_5)_2 + H_2O \rightarrow ZnO + 2C_2H_6}.$$

ALD processes were performed using the Savannah-100 reactor from Cambridge NanoTech. We explored films deposited at temperature between 100 ℃ and 300 ℃, which are inside temperature limits required for the 3D electronics. As substrates we used glass, silicon and commercial $\mathrm{GaN/Al_2O_3}$ substrates.

3. Results and discussion

Atomic force microscopy (AFM) studies showed that obtained ZnO films were atomically flat. The root mean square (rms) of a surface roughness depends on deposition temperature and layer thickness as we already reported [7]. The rms value does not exceed 1 nm for films with thickness of 100 nm and less, which is typical thickness used for electronic application.

The XRD investigations performed with the X'Pert MPD diffractometer in a full angular range show that films grown at temperatures between 100 ℃ and 200 ℃ are polycrystalline. The preferred crystallographic orientation depends on growth temperature, pulsing time of each of precursors and purging time [7]. Therefore we were able to choose such growth conditions which privilege ZnO growth with c axis perpendicular to the surface. In this way we obtained films that show only one 00.2 peak in the XRD spectrum as it is shown in Fig. 1a.

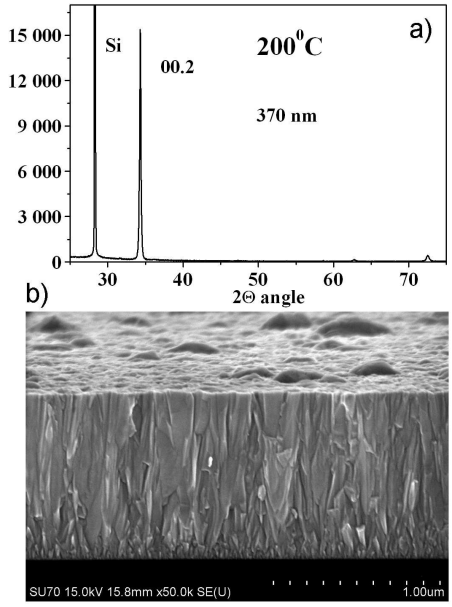

Fig. 1. (a) The XRD spectrum of the polycrystalline ZnO film with c axis perpendicular to the surface. (b) The SEM image of a low temperature polycrystalline ZnO film.

Polycrystalline films are uniform and show the columnar type of growth as is illustrated at a scanning electron microscopy (SEM) image of the ZnO film cross-section in Fig. 1b. The column width depends on the film thickness and varies between 15 and 20 nm for thin films (100 nm thick and less), and between 40 and 50 nm for films of 0.4 μm thickness.

ZnO films grown on a commercial $\mathrm{GaN/Al_2O_3}$ substrates at temperature of 250 ℃ and higher, are monocrystalline as was confirmed by a high resolution X'Pert MRD diffractometer equipped with the X-ray mirror, a four-bounce monochromator at the incident beam and a three bounce analyzer at the diffracted beam (Fig. 2a). The full width at half maximum (FWHM) rocking curve of 00.2 reflection measured with analyzer was 230 arcsec for layers grown at 280 ℃ and 250 arcsec when growth temperature was 300 ℃. These values are

very close to that measured for a gallium nitride template which means that GaN substrate and ZnO layers have similar number of screw dislocations. The rocking curve of the asymmetrical peak 20.1 is much larger for the ZnO layer (2230 arcsec) than for the GaN deposited on Al_2O_3 substrate (640 arcsec), which means that ZnO layer has higher concentration of edge dislocations (see Fig. 2b).

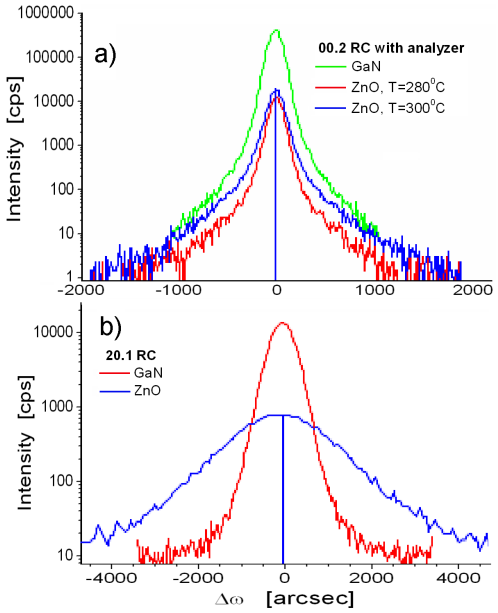

Fig. 2. The comparison of the rocking curve of the monocrystalline ZnO films grown at 280 °C (S396) (a) with a rocking curve of a GaN/Al_2O_3 substrate (b).

A value of free electron concentration is an important parameter closely related to application of zinc oxide in electronic devices. Conductivity of ZnO strongly depends on the growth conditions and ranges from metallic to insulating. Consequently, the n electron concentration in this material is usually reported from 10^{17} to 10^{21} cm^{-3} for "as grown" film depending on the growth method used [13, 14]. A high level of unintentional doping in nominally undoped ZnO is related to a number of intrinsic defects attributed to zinc interstitial, oxygen vacancies, zinc vacancies and hydrogen contamination [15–17].

We obtained electrical properties of zinc oxide films grown by ALD from the Hall effect measurements in the van der Pauw configuration using the RH2035 Phys-Tech GmbH system. For polycrystalline films we have found a very clear relation between a free electron concentration and growth temperature. We observed that electron concentration for films deposited at temperature of 100 °C and lower was at the level of 10^{17} cm^{-3} while it was 10^{20} cm^{-3} for films deposited at 240 °C. The values of a free electron concentration for samples grown at various temperature with the same pulsing and purging time are gathered in Table I. We expect that lower electron concentration at reduced growth temperature is observed because formation of defects like oxygen or zinc vacancies require some activation energy. Therefore the number of defects should be suppressed at lower deposition temperature. Electron mobility μ in polycrystalline ZnO films was relatively high. We obtained the μ value between 10 and 50 cm^2/(V s), which is relatively high value taking into account that growth temperature was between 100 °C and 200 °C and that films are polycrystalline. This value is also not very different from that obtained for the bulk monocrystalline zinc oxide (250 cm^2/(V s)). Electrical properties of polycrystalline zinc oxide films grown at 100 °C are very close to fulfill requirements of a material which can be used for electronic devices as theoretical modeling shows [18] that electron mobility of ZnO used for a Schottky diode should not be lower than 10 cm^2/(V s), while free electron concentration should not exceed 2×10^{17}/ cm^3.

TABLE I
Electrical parameters of polycrystalline zinc oxide films deposited on glass. ZnO films were grown using the same parameters (pulsing and purging time).

Growth temperature [°C]	n concentration [cm^{-3}]	Mobility [cm^2/(V s)]	Conductivity [Ω^{-1} cm^{-1}]
100	4.5×10^{17}	8	0.58
140	7.0×10^{18}	38	42.6
200	1.7×10^{20}	16	431.0

We used a unique approach to achieve electrical parameters appropriate for the Schottky junction applications. We optimized growth conditions of the ALD process (e.g. pulsing and purging time after each precursor) in order to obtain films with both low electron concentration and low intensity of defect-related photoluminescence (PL) bands.

Our polycrystalline ZnO films grown between 60 °C and 200 °C show band-edge PL even at room temperature (RT). They also show defect-related PL bands situated in green, red and yellow parts of the spectra. The presence of these bands is attributed to defect levels, usually abundant in ZnO films. We expect that films with low intensity of defect-related bands have also a lower number of defects and thus low free carrier concentration is not a result of the compensation effect.

Room temperature PL of two ZnO films grown at 100 °C with different ALD process parameters (e.g. before and after optimization) is shown in Fig. 3. Free carrier concentration of the films grown at 100 °C and showing very low PL defect-related bands was at the level of 5×10^{16} cm^{-3}. In this way we obtained zinc oxide films with electrical properties fulfilling theoretical requirements for a Schottky junction. Based on these optimized low temperature ZnO films and silver we were able to build thin film transistor with I_{on}/I_{off} ratio of 10^7 at 1.5 V and a forward current density of 10^4 A/cm^2 as we reported before [10, 19].

Electrical parameters of monocrystalline ZnO films grown on a commercial GaN/Al_2O_3 substrate at temper-

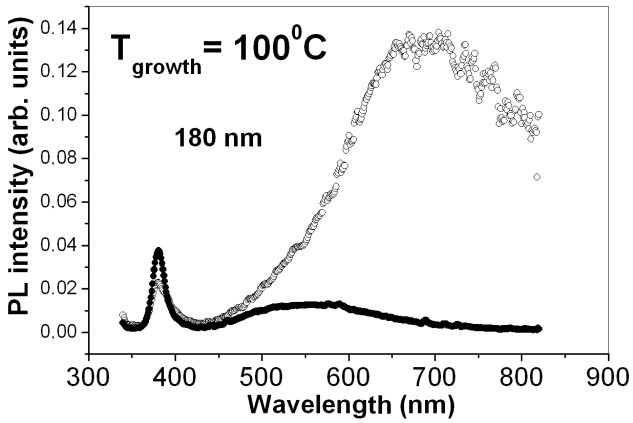

Fig. 3. Room temperature photoluminescence spectra of ZnO films grown at 100 °C before (open circles) and after optimization (solid circles).

TABLE II

Electrical parameters of monocrystalline zinc oxide films deposited on GaN/Al_2O_3 substrate. ZnO films were grown using the same parameters (pulsing and purging time).

Growth temperature [°C]	n concentration [cm^{-3}]	Mobility [$cm^2/(V\,s)$]	Conductivity [$\Omega^{-1}\ cm^{-1}$]
250	1.3×10^{19}	30.0	62.5
280	8.6×10^{18}	34.5	47.4
300	1.3×10^{19}	31.6	67.8

ature between 250 °C and 300 °C are gathered in Table II. Electron mobility of these films is comparable or higher than that of polycrystalline ones and exceeds 30 $cm^2/(V\,s)$. Unfortunately, n electron concentration values were measured between 8×10^{18} and 2×10^{19} cm^{-3}, which is too high for a ZnO Schottky junction application. However, these values are at least two orders of magnitude lower than that obtained for polycrystalline zinc oxide films grown at comparable temperature. The investigations on the source of defects in both poly- and monocrystalline ZnO films are in progress.

4. Summary

Using atomic layer deposition and diethylzinc and water precursors, we obtained polycrystalline ZnO thin films with high mobility and low free electron concentration. Electrical parameters and deposition temperature at the level of 100 °C imply application of these films for the Schottky junctions dedicated for a 3D electronics. Monocrystalline ZnO films with FWHM of the 00.2 diffraction peak equal to 230 arcsec were obtained at temperature above 300 °C. Free carrier concentration in monocrystalline ZnO layers was found between 8×10^{18} and 2×10^{19} cm^{-3}, which is too high for a ZnO Schottky junction application.

Acknowledgments

The research was partially supported by European Union within the European Regional Development Found, through Innovative Economy (POIG.01.01.02-00--008/08) and Polish Ministry of Science and Higher Education — project No. 0663/B/T02/2008/35.

References

[1] G. Moore, *Electronics* **38**, 4 (1965).

[2] K. Ishimaru, *Solid-State Electron.* **52**, 1266 (2008).

[3] G.D. Wilk, R.M. Wallace, J.M. Anthony, *J. Appl. Phys.* **89**, 5243 (2001).

[4] M. Johnson, A. Al-Shamma, D. Bosch, M. Crowley, M. Farmwald, L. Fasoli, A. Ilkabar, B. Kleveland, T. Lee, Liu Tz-yi, N. Quang, R. Scheuerlein, K. So, T. Thorp, *IEEE J. Solid State Circ.* **38**, 1920 (2003).

[5] S. Wagner, H. Gleskowa, I.-Ch. Cheng, M. Wu, *Thin Solid Films* **430**, 15 (2003).

[6] R. Triboulet, J. Perrière, *Prog. Cryst. Growth Charact. Mater.* **47**, 65 (2003).

[7] I.A. Kowalik, E. Guziewicz, K. Kopalko, S. Yatsunenko, A. Wójcik-Głodowska, M. Godlewski, P. Dłużewski, E. Łusakowska, W. Paszkowicz, *J. Cryst. Growth* **311**, 1096 (2009).

[8] V. Craciun, J. Elders, J.G.E. Gardeniers, I.W. Boyd, *Appl. Phys. Lett.* **65**, 2963 (1994).

[9] E. Guziewicz, I.A. Kowalik, M. Godlewski, K. Kopalko, V. Osinniy, A. Wójcik, S. Yatsunenko, E. Łusakowska, W. Paszkowicz, M. Guziewicz, *J. Appl. Phys.* **103**, 033515 (2008).

[10] N. Huby, S. Ferrari, E. Guziewicz, M. Godlewski, V. Osinniy, *Appl. Phys. Lett.* **92**, 023502 (2007).

[11] M. Godlewski, E. Guziewicz, G. Łuka, T. Krajewski, M. Łukasiewicz, Ł. Wachnicki, A. Wachnicka, K. Kopalko, A. Sarem, B. Dalati, *Thin Solid Films*, in press.

[12] E. Katsia, N. Huby, G. Tallarida, B. Kutrzeba-Kotowska, M. Perego, S. Ferrari, F.C. Krebs, E. Guziewicz, M. Godlewski, V. Osinniy, G. Luka, *Appl. Phys. Lett.* **94**, 143501 (2009).

[13] S.K. Kim, C.H. Hwang, S.H.K. Park, S.J. Yun, *Thin Solid Films* **478**, 103 (2005).

[14] S.H.K. Park, C.S. Hwang, H.S. Kwack, J.H. Lee, H.Y. Chu, *Electrochem. Solid-State Lett.* **9**, G299 (2006).

[15] E.G. Bylander, *J. Appl. Phys.* **49**, 1188 (1978).

[16] K. Vanheusden, C.H. Seager, W.L. Warren, D.R. Tallant, J.A. Voiget, *Appl. Phys. Lett.* **68**, 403 (1996).

[17] M. Liu, A.H. Kitai, P. Mascher, *J. Lumin.* **54**, 35 (1992).

[18] M. Prà, S. Schuster, C. Erlen, G. Csaba, P. Lugli, in: *Emerging Non-Volatile Memories, ESSDERC 2007*, München 2008.

[19] N. Huby, G. Tallarida, M. Kutrzeba, S. Ferrari, E. Guziewicz, Ł. Wachnicki, M. Godlewski, *Microelectron. Eng.* **85**, 2442 (2008).