

The Design Aspects for Ultra Low-Power, Low-Noise 90 nm CMOS Charge Sensitive Amplifier for the Active Pixel Detector

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A falling particle in the digital registration systems for elementary particles active pixel detector induces electric charge, the value of which describes the parameters of the particle in the detector. Since the electric charge induced by a single particle is relatively weak, the detector signal is first processed (amplified and shaped) right in the zone of irradiation and only then transmitted further. This paper analyses the primary analogical registration electronics for digital registration systems for elementary particles active pixel detectors, which is charge sensitive amplifiers operating in the nanoampere region.

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1. Introduction

The charge created by the interaction of the high energy particles in the sensor is very small and has to be amplified in a low-noise, very low power circuit before any further signal processing. The signal induced on the electrodes of the sensor is transferred to the readout chip, where it is integrated and amplified in a charge sensitive amplifier (CSA) [1, 2]. The amplifier design is critical since it should match the detector interface. The front-end chips are fabricated in state-of-the-art industrial silicon CMOS or GaAs MESFET processes [3, 4]. This allows more logic to be introduced into a pixel or the use of a smaller pixel size. In particular, the low power and high integration of the CMOS 90 nm technology make it an attractive choice for the implementation of low noise front-end electronics in high resolution imaging detection systems.

2. The design aspects for ultra low-power, low-noise CMOS charge sensitive amplifier

It is useful to express the noise sources as an equivalent noise charge (ENC) at the amplifier input. The ENC depends on the detector capacitance C_{det} , on the detector leakage current I_{leakage} , on the input FET capacitance C_{in} and series noise (including both thermal and flicker noise).

Attention must be paid to the minimization of the CSA capacitance and the detector leakage current, because ENC depends on these parameters. Problems with the leakage current become crucial especially after irradiation, which yields as high as a few nanoamperes of cur-

rent flowing into the input of the readout system. Therefore, it is necessary to minimize this influence. Figure 1 shows the scheme of the simplified structure of the proposed CMOS CSA with automatic leakage current compensation for digital registration systems for elementary particles (DRSEP). This configuration provides a constant current fast return to zero through the transistors T_{4A} and T_{4B} controlled by the $2I_p$ current. The input node is therefore discharged with a net current of I_p , independent of the leakage current I_{leakage} . The current in the leakage compensation device T_{6A} is regulated so that it equals $I_{\text{leakage}} + I_p$ in the equilibrium state. So, the detector leakage current (dc component) flows into T_{6A} rather than into the equivalent feedback resistance R_{fb} , which is implemented by PMOS transistors T_{4A} and T_{4B} . By using the 8-bit DAC with the current output for the control of the leakage current compensation circuit, 255 possible CSA $2I_p$ current combinations can be commutated, i.e. from 0 nA to 255 nA, every 1 nA. Such control of the leakage current compensation circuit $2I_p$ would cover a wide leakage current band and would allow reduction of CSA ENC.

The operational amplifier consists of a pair of n -channel transistors for the input T_{1A} and T_{1B} , driving a p -channel (T_{3A} , T_{3B}) current mirror stage as active load and a pair of n -channel cascade (T_{2A} , T_{2B}) transistors depress the Miller effect at the input and improve the gain factor of the amplifier. The Miller effect makes that the input capacitance C_{in} seems significantly larger than just the capacitance C_{gs} of the input transistor T_{1A} . C_{in} must be low, because it plays a crucial impact on the CSA peaking time, the signal-to-noise ratio and band-limits.

The transistor T_{5A} is placed in a pixel CSA and the diode connected transistor T_{5B} , which is biased by the output current of a DAC, make together a current mirror. This circuit uses about 500 nA bias current I_{bias} from the

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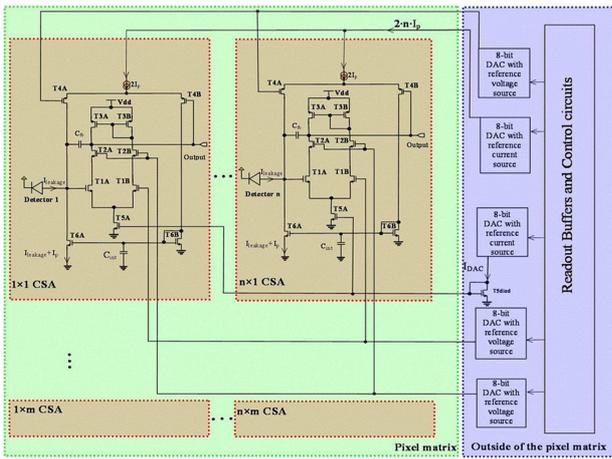


Fig. 1. Simplified structure of the proposed analog electronics architecture for the DRSEP active pixel detector.

$V_{dd} = 1$ V power supply source and the total power P_{tot} of about 500 nW.

3. Simulation results

The circuit was implemented with a 90 nm CMOS technology manufactured at IBM [4]. Computer simulation has been performed with the Simulation Program with Integrated Circuit Emphasis (SPICE) simulator. The SPICE simulation of the charge sensitive amplifier is performed using the BSIM4, BSIM3 V3 models of this technology process. The simulations were performed for one channel, including the electrical model of the transmission line between the detector and the CSA. In order to test the response of the CSA to an injected charge pulse, or a train of charge pulses, a known charge pulse

was injected into the CSA. The simulation of the CSA is optimized for a CdZnTe detector, because this material has the high atomic number and gives high detection efficiency relative to Si. The output response for the 90 nm CSA at the input charge equal to $1 \text{ k}\bar{e}$ (160 aC), is presented in Fig. 2a for detector capacitance $C_{det} = 30 \text{ fF}$. The CSA output signal is a semi-Gaussian pulse form with exponential a rise time constant and a decay long time constant. Figure 2b shows the peaking time versus detector capacitance. The simulation shows the peaking time of 25 ns at the 0 fF input capacitance and a strong dependence on the detector capacitance. The expected peaking time for 300 μm thick CdZnTe detector ($C_{det} = 30 \text{ fF}$) for the amplifier is about 45 ns, charge-to-voltage gain is about $71 \text{ mV/k}\bar{e}$. In all sense, the amplifier has unipolar response. Each amplifier dissipates $0.5 \mu\text{W}$ power.

4. Conclusions

A new DRSEP active pixel detector (APD) analog electronics architecture allowing reduction of the detector leakage current and CSA noises as well as control of the charge-to-voltage gain, offset voltage, operating current and the used power has been proposed. The nanometric 90 nm 90SRF technology CSA with the leakage current compensation circuit using very low power of about 500 nW with the quality function equal to $80 \mu\text{W}\bar{e}$ has been designed. Other main parameters of CSA are the following: the unipolar output signal with the peaking time τ_p of about 35–40 ns, the transfer coefficient of 60–90 $\text{mV/k}\bar{e}$, the output signal nonlinearity 1–5 $\text{k}\bar{e}$ in the input signal range is about 1.6%, and the equivalent noise charge, when the input signal Q_{det} is in the 1–10 $\text{k}\bar{e}$ range and the detector capacitance $C_{det} = 30 \text{ fF}$, is lower than $160 \bar{e}$.

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References

- [1] G. Batignani, S. Bettarini, F. Bosi, *Nucl. Phys. B (Proc. Suppl.)* **172**, 20 (2007).
- [2] V. Barzdenas, R. Navickas, *Solid State Phenom. Mechatronic Syst. Mater. MSM 2005* **113**, 453 (2006).
- [3] V. Barzdenas, R. Navickas, *Acta Phys. Pol. A* **113**, 825 (2008).
- [4] MOSIS, *Integrated Circuits Fabrication Service*: <http://www.mosis.org>.

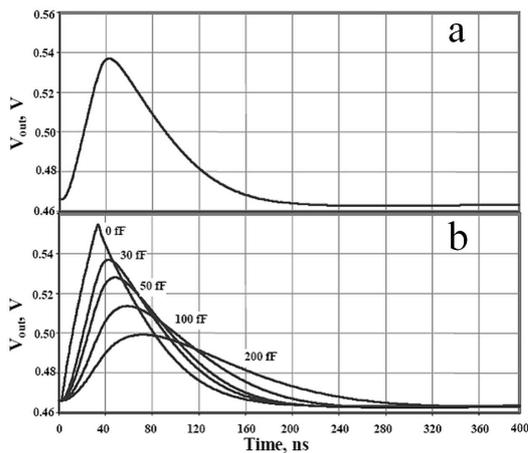


Fig. 2. Simulation results: (a) simulations of the 90 nm CSA output waveform of injected charge ($Q_{det} = 1 \text{ k}\bar{e}$, $C_{det} = 30 \text{ fF}$, $T_{ap} = 27^\circ\text{C}$, CdZnTe detector); (b) real signal response of the 90 nm CSA for different input capacitance ($Q_{det} = 1 \text{ k}\bar{e}$, $T_{ap} = 27^\circ\text{C}$, CdZnTe detector).