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Formation of Nanostructured Layers for Passivation of High Power Silicon Devices

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Nanocrystalline porous silicon films, which have been formed by using simple wet electrochemical etching process in HF electrolyte, were applied for passivation of high power silicon diodes. An optimal technology was designed to manufacture a uniform layer of porous silicon over the area of the $p-n$ junction. The 8% increase in the yield was achieved on Ø100 mm diameter wafers with 69 cells of diodes in each, by using a very simple technology for the formation of porous layer for passivation of high power silicon diodes.

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1. Introduction

Thin dielectric passivation layers are basic construction elements in semiconductor device technology. The layers are mainly oxides, SiO_2 being the most popular of them, although the phosphor- and boron-silicon glasses are used as passivation layers, too [1]. In choosing a passivant for power thyristors and diodes, there are two important factors in addition to the usual requirement for providing uniform high breakdown voltage. One is related to thermal stability of the passivant to subsequent high-temperature processes. The other is the bias-temperature stability of the passivation layers which affects the operation lifetime of a device [2, 3].

In this work a new passivation scheme is proposed which is based on a formation of nanostructured layer for passivation of the surface of space charge region. This work is focused on the development of a simple technique for a rapid formation of porous silicon layer as a passivation coating for typical crystalline silicon industrial power thyristors and diodes structures.

2. Experimental

High-power thyristors and diodes were formed by diffusion technique using n-Si (111) wafers of Ø100 mm and resistivity of (75–120) Ω cm. In the wafer, the thyristors/diodes were separated by grooves of ≈ 100 μm in depth and 800 μm

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in width etched by HF:HNO_3: H_3COOH solutions. Using a standard technology, the surface of the p–n junctions were passivated by filling the grooves with glass (SiO_2–PbO–Al_2O_3–B_2O_3) powder melted at (750–760)°C, Fig. 1.

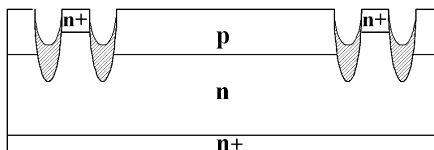

Fig. 1. The cross-section of the diode structure.

In the proposed technology, the p–n junction at the surface of grooves was passivated by porous silicon layers before glass-filling procedure. Porous silicon layers were formed electrochemically in fluoroplastic cell. The diode structures were etched in HF:C_2H_5OH (1:1) electrolyte at electric current density (20–30) mA/cm^2 and etching time (20–180) s. The etching process was carried out in galvanostatic regime by means of AUTOLAB, GPES-General Purpose Electrochemical System. As the anodized area contained the p–n junctions, i.e., the p- and n-type regions were etched simultaneously, the etched surface was illuminated by 100 W incandescent lamp ($\lambda = 1.12$ μm, 600 lx). After electrochemical process, the passivated diode structures were washed by distilled water, dried and annealed at 550°C in hydrogen atmosphere. The surface morphology was investigated by means of electron microscope BS 300 and atomic force microscope Thermomicroscope Explorer.

3. Results and discussion

The morphology of the diode structure prepared by standard technology is illustrated in Fig. 2. It is seen (Fig. 2b) that the glass has coated the groove non-homogeneously. In addition, the bulk glass is porous, which favors adsorption of water and vapor in the ambient atmosphere. These factors deteriorate the characteristics of high power diode structures. It is known [2] that the passivation of p–n junction by glass causes the hydrogen desorption leading to an increase in dangling bonds at the Si-glass interface and decrease in breakdown voltage. The formation of porous silicon layer is expected to passivate free Si bonds by supplying hydrogen [4].

The next factor influencing the breakdown voltage is the presence of metal ions on the surface of p–n junction. The metal ions are adsorbed during the chemical processes for example during etching of grooves in acid solutions. An increase in HF concentration leads to the increase in adsorption of metal ions. When HF concentration is 1.2 M, the concentration of adsorbed metal ions is 5×10^{15} cm^{-2} [5]. An increase in HNO_3 concentration favors the oxidation of metal ions and solution of metal oxides. Adding acetic acid to etching solution allowed us to lower the concentration of adsorbed Fe, Ni, Co, Cd ions down to 5×10^{13} cm^{-2}. In

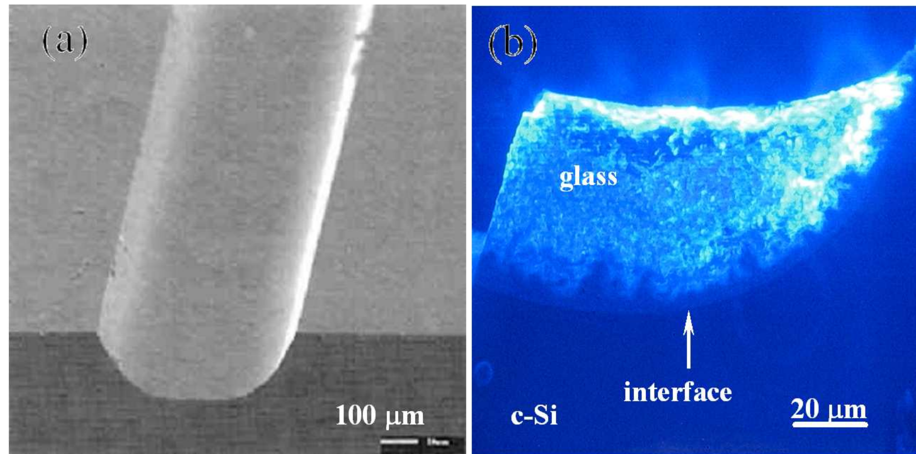

Fig. 2. The scanning electron microscopy (SEM) micrograph of standard diode structure before (a) and after (b) filling with glass in the region of groove. The p–n junction is located at 35 μm from the wafer surface; the groove depth is 95 ± 5 μm.

addition, the porous silicon layer is known [6, 7] to possess the gettering feature. Therefore, it is reasonable to predict that passivation of p–n junction by porous silicon before glass-filling procedure will improve the characteristics of diode structures. It should be also emphasized that another important property of porous silicon is the gettering of the structural defects like dislocations, leading to an increase in average yield of diode structures in industrial silicon wafers [7].

The cross-section of diode structure along the groove is shown in Fig. 3. Figure 4 shows that a quite uniform porous silica layer of thickness $d \approx 7$ μm is formed which is narrower in p-type region and wider (more diffuse) in n-type side. The thickness can be controlled by etching period (Fig. 4) and current density [8]. A slight difference in porous silicon layer on the two sides of p–n junction is caused by different etching mechanism [9]. The transition between porous layers on p- and n-type sides of diode structures is achieved due to IR illumination.

The passivation quality of diode structures has been controlled by measurements of surface recombination characteristics determined by non-invasive technique which employed microwave probed photoconductivity transients (MW-PCT). It has been revealed that the passivation of the structures by the formation of porous silicon layers before glass melting resulted in a decrease in surface recombination velocity from 3×10^3 cm/s to 10 cm/s.

Breakdown tests on diodes has shown that the passivation by porous silicon layer has increased the average breakdown voltage (Table) and an increase in yield of 8% was obtained on three Ø100 mm wafers with 69 cells of diodes in each. In conclusion, nanocrystalline porous silicon film were used for passivation of p–n junction surface of high power silicon devices. The passivation has allowed to increase the breakdown voltage by about 8%.

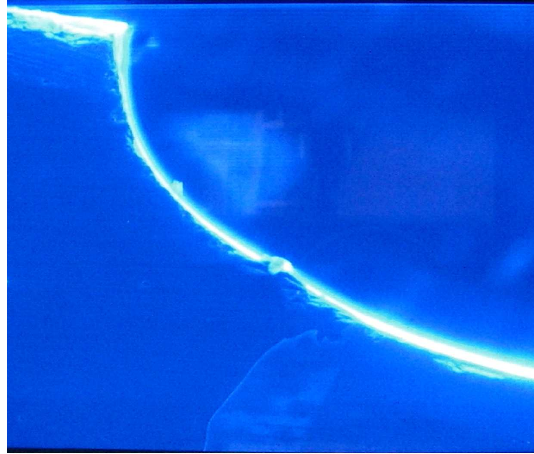

Fig. 3. SEM micrograph of the cross-section of diode structure along the groove passivated by porous silicon formed at etching for 1 min in $HF:C_2H_5OH$ (1:1) electrolyte at current density 30 mA/cm^2.

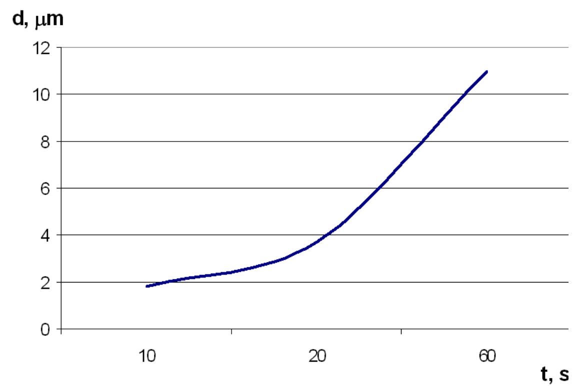

Fig. 4. Dependence of the thickness of porous silicon layer on etching time in $HF:C_2H_5OH$ (1:1) electrolyte at current density 30 mA/cm^2.

TABLE

Averages of U_{rrm} (reverse repetitive maximum) values of diode structures without (a) and with (b) passivation by porous silicon layer.

Wafer number	1	2	3
U_{rrm} [V], (a)	1860.9	1807.2	1766.7
(b)	1909.6	1847.2	1900.0

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