Electron Charge Noise Minimization in 130 nm CMOS Preamplifiers

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In this paper we present the design aspects for low-power, low-noise CMOS charge sensitive preamplifier that uses a leakage current compensation circuit for use with radiation sensors. The preamplifier has unipolar response with the peaking time of about 45 ns and the gain about 115–145 mV/ke. Equivalent noise charge (ENC) is less than 80 e, when the input charge is 1–20 ke and the sensors capacitance is equal to 30 fF. In this work we present the quality function of the charge sensitive preamplifier, which characterizes best the optimal input transistor width W, with respect to equivalent noise charge and to the power consumptions.

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1. Introduction

Submicron CMOS technologies ensure radiation hardness required by detector readout systems in present high-energy physics experiments as well as in other application fields [1]. The charge created by the interaction of the high energy particles in the sensor is very small and has to be amplified in a low–noise, very low power circuit before any further signal processing. The signal induced on the electrodes of the sensor is transferred to the readout chip, where it is integrated and amplified in a charge sensitive preamplifier (CSP) [2]. The preamplifier design is critical since it should match the detector interface.

2. Investigated devices

We have received transistor-models based on the commercial 130 nm CMOS technology from IBM company [3]. The oxide thickness T_{ox} was 24 Å, the gate capacitance per unit area C_{ox} was about 14.8 fF/μm^2 and the maximum allowed supply voltage V$_{dd}$ was +1.2 V. We studied devices with a different gate length L ranging from 0.13 to 1 μm and with a gate width W ranging from 0.64 to 12 μm.

3. CSP with leakage current compensation

Attention must be paid to the minimization of CSP capacitance and the detector leakage current, because equivalent noise charge (ENC) depends on these

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parameters [4]. Problems with the leakage current become crucial especially after irradiation by particle, which yields as high as a few nanoamperes of current flowing into the input of the readout system. Therefore, it is necessary to minimize this influence. Figure 1 shows the schematic of the simplified structure of
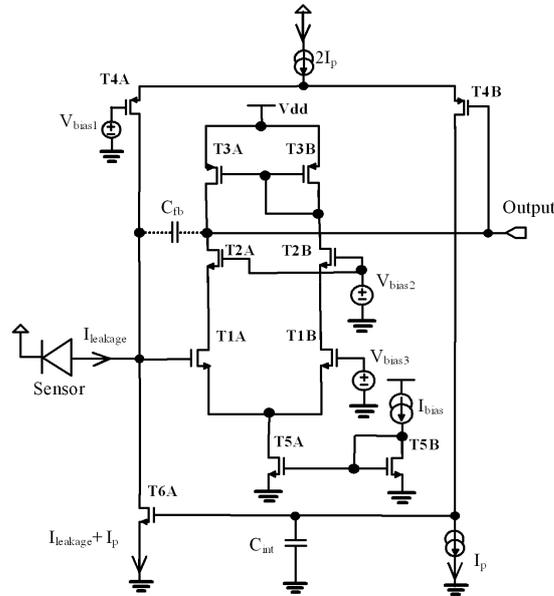

Fig. 1. Simplified structure of a CMOS preamplifier with automatic leakage current compensation.

a CMOS preamplifier (CSP) with automatic leakage current compensation. The idea of current compensation method lying at the background of this article has been borrowed from Ref. [5]. This configuration provides a fast return of constant current to zero through the transistors T2A and T2B controlled by the $2I_\mathrm{p}$ current. The input node is therefore discharged with a net current of I_p, independent of the leakage current I_leak. The current in the leakage compensation device T6A is regulated so that it equals $I_\mathrm{leak} + I_\mathrm{p}$ in the equilibrium state. Therefore, the detector leakage current (dc component) flows into T6A rather than into the equivalent feedback resistance R_fb, which is implemented by PMOS transistors T4A and T4B.

4. ENC minimization and simulation results

It is well known that the best transistor width for optimizing the resolution must exist at which the flicker $(1/f)$ noise and the transistor channel noise contribution, is minimal [4]. The gate width W of input transistor has a double effect. On the one hand, the increase in the gate width impairs the ENC ratio due

to the increase in the input capacitance. On the other hand, the increase in the gate width reduces the transistors channel thermal noise due to the increase in the transistor transconductance and the power consumption. The power consumption P of the CSP must be kept very low, because the matrix of readout cells consists of a large number of pixels.

The optimal W must be found by solving the following set of equation:

$$Q(W) = \text{ENC}(W)P(W), \tag{4.1}$$

where $\text{ENC}(W)$ is the geometric sum of the flicker $(1/f)$ noise and transistor channel noise contribution, $P(W)$ is power consumption versus the input transistor channel. The idea for these function calculations had been borrowed from Refs. [2, 4, 5]. $Q(W)$ is the quality function of the CSP. This function is quadratic with one minimum and characterizes the optimal/ best W, depending on the ENC and the power consumptions (see Fig. 2). When $Q(W)$ function is in the range from 1 μm to 1.5 μm, then it is minimal and is about 4 μW e. This range was estimated in the design of the CSP.
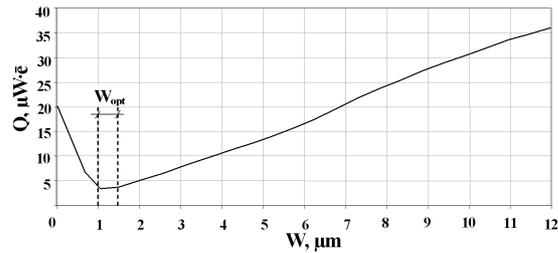

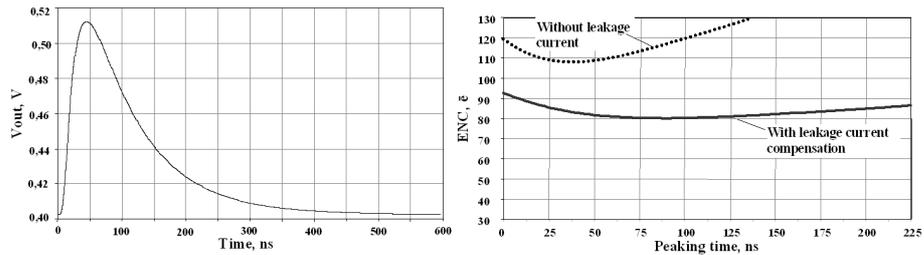Fig. 2. Theoretical quality function Q of the CSP versus the input transistor channel width W.

Fig. 3. Simulations results of the preamplifier: a) real signal response of the preamplifier ($Q_{\text{in}} = 1$ ke, $C_{\text{det}} = 30$ fF); (b) the total ENC as a function of peaking time.

Figure 3a shows the simulated pulse response for CSP. The detector signal is modelled as a delta current pulse. The circuit modeling for Simulation Program with Integrated Circuit Emphasis (SPICE) simulation includes the electrical model of the transmission line between the detector and front-end. The input signals

Q_{in} = 1000 ke (0.16 fC), with the applied 30 fF capacitor at the preamplifier input. Figure 3b presents the simulation results of the total ENC contributions as a timing resolution with and without leakage current compensation. This function of CSP without the leakage compensation is quadratic, concave with one minimum, which is adequate for ENC minimum, ENC = 108 e, when peaking time is about 45 ns. ENC of the CSP with leakage current compensation decreases down to 80 e and lines the right side of this function.

5. Conclusions

We have designed a high-speed CMOS preamplifier with the leakage current compensation circuits using 130 nm IBM technologies. Noise minimization of the charge sensitive preamplifier at input stages has been performed. The preamplifier has unipolar response with the peaking time of about 45 ns and the gain in the range 6115–145 mV/ke, very low-power consumption of 1.2 μW/preamplifier and equivalent noise charge ENC of less than 80 e, when the detector capacitance is equal to 30 fF.

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