

Blue Optoelectronics in III–V Nitrides on Silicon

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Three simple and promising methods to grow high-quality, device-relevant gallium nitride heterostructures on silicon are presented: strain-compensation, patterning, and the insertion of low-temperature AlN interlayers. With all methods device-quality GaN can be grown. While patterning is especially interesting for light emitters, low-temperature AlN interlayers can be used universally not only for transistor structures, which require good insulation of the active layers to the Si substrate, but also for vertically contacted LEDs when doped with Si. Low-temperature AlN interlayers do not only reduce tensile stress but also improve GaN properties and strongly reduce the threading dislocation density from 10^{10} cm^{-2} to 10^9 cm^{-2} for 2 low-temperature AlN layers. Additionally, the layer quality can be enhanced by using *in situ* Si_xN_y masks. Best crack-free layers with dislocation densities around 10^9 cm^{-2} show X-ray rocking-curve widths around 400 arcsec and narrow photoluminescence. So far, best LEDs on Si(111) have an optical output power of 0.42 mW at 20 mA and 498 nm which is enough for simple signal applications.

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1. Introduction

With the achievement of *p*-type doping in group-III nitrides in the late 80's a fast progress in growth and device development was initiated [1]. In spite of large efforts there is still a lack of available homosubstrates. The technology for the growth of large bulk single-crystal GaN substrates still remains to be developed and therefore large-scale homoepitaxial growth of GaN/GaN will not be possible in the near future. Currently, GaN-based devices are usually grown on transparent sapphire or silicon carbide substrates. These are either insulating or very expensive and not available in large diameter. Silicon is the substrate of choice for the

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integration of optoelectronics or high-power electronics with Si-based electronics because of its cheapness, availability of large and high-quality substrates combined with good thermal conductivity and insulating or conductive electrical properties. In addition, Si substrates are also interesting for the cheap production of devices as light emitters and transistors. The main problem hindering the progress of GaN growth on silicon is the thermal mismatch of GaN and Si leading to tensile stressed layers and cracks even below device-relevant layer thicknesses. In the last few years, since the first demonstration of a (MBE grown) GaN-based LED on Si in 1998 [2] the activities in research of GaN on Si increased dramatically. Meanwhile several concepts to lower stress, avoid cracks, and improve the material quality exist. In contrast to GaAs- or InP-based devices, GaN-based devices are known to operate very well without aging effects with dislocation densities as high as 10^{10} cm^{-2} . Thus, the integration of Si- and GaN-based devices on the same chip becomes feasible as well as a silicon-based optoelectronics technology, e.g. with the potential for small, high resolution, full color displays. Meanwhile, the material quality is approaching that on sapphire, so that it is only a question of time until GaN-based devices on Si will come into market. Actually, a US company, Nitronex inc., has already started strong market activities [3]. This article gives an overview on the latest developments in metal organic chemical vapor phase epitaxy (MOVPE) group-III nitride growth on Si. Additional information can be found in a recent review article [4].

2. The strain problem

Strain engineering is the key to achieve high-quality device structures on Si. Besides the cracks mentioned above, the film stress exerts a bending moment on the substrate leading to a substrate curvature, which is also important for device processing since a small radius of the wafer curvature is problematic in processing, e.g. in contact lithography. The problem can be addressed to as follows: below the critical thickness, a homogeneous perfect, epitaxial (0001)-oriented thin GaN film on AlN/silicon would be under biaxial stress. Under these conditions for the strains the relation holds

$$\varepsilon_3 = -2(C_{13}/C_{33})\varepsilon_1$$

$\varepsilon_3 = (c - c_0)/c_0$ and $\varepsilon_1 = (a - a_0)/a_0$, with (a, c) and (a_0, c_0) being the lattice constants of the strained and fully relaxed layer, respectively. C_{ij} are the stiffness coefficients. The factor $p = \varepsilon_3/\varepsilon_1 = -2(C_{13}/C_{33})$ is related to the Poisson ratio ν by $p = -2\nu/(1 - \nu)$ or $\nu = -p/(-2 + p)$. Unfortunately, the published values on the elastic constants strongly differ from each other, the reported experimental and calculated values for ν range from 0.20 to 0.37 [5, 6], whereby the value of $\nu = 0.20$ calculated by Wright from density functional theory [5] is in excellent agreement with the experimental value of $\nu = 0.23 \pm 0.06$ [6].

Although the stress due to the lattice mismatch can be nearly completely relaxed within the first nanometers, there is always thermal stress, which occurs during the cooling process after the growth at high temperature due to the difference in the linear thermal expansion coefficients. In equilibrium, the bending moments of the film and the substrate equal each other. Assuming isotropic film stress σ_f and a spherical shape the film stress is related to the radius of curvature, R_{exp} [7]:

$$\sigma_f = \frac{E_s t_s^3 + E_f t_f^3}{6(1 - \nu_f)(t_s + t_f)t_f R_{\text{exp}}},$$

$E_{s,f}$ being the Young moduli of substrate and film, $t_{s,f}$ — the substrate and film thicknesses, and ν_f — the Poisson ratio of the film. In the case $t_f \ll t_s$, the relation reduces to

$$\sigma_f = \frac{E_s t_s^2}{6(1 - \nu_f)t_f R_{\text{exp}}}.$$

The situation is schematically shown in Fig. 1. In case of a compressively strained film, either due to the lattice mismatch or the thermal mismatch, the bent system will show a convex film surface, in case of a tensily strained film, the film surface will be of concave shape. The first situation arises for thick GaN on sapphire samples because the thermal expansion coefficient of GaN is smaller than that of sapphire or for GaN on AlGaIn due to the lower in-plane lattice constant of AlGaIn. Therefore, a biaxial compressive stress is induced in the GaN. A concave shaped surface is observed e.g. for GaN on silicon samples because the thermal expansion coefficient of GaN is higher than that of silicon and a biaxial tensile stress is induced in the GaN. With increasing film thickness, the bending increases.

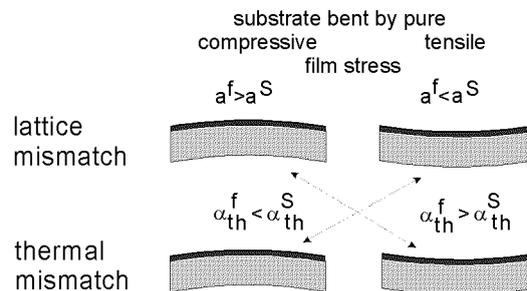


Fig. 1. Compressively or tensily strained films lead to a convex or concave film surface.

The radius of curvature can be measured easily, e.g. by X-ray diffraction techniques. When a curved sample is mounted on a translational stage of an X-ray spectrometer the angle of incidence of the X-ray beam changes as the wafer is translated. The radius of curvature can be calculated from the measured orientation difference $\Delta\omega$ of a set of lattice planes separated by l . The radius of curvature

is then given by $R_{\text{exp}} = 180 / (\pi \Delta\omega)$, $\Delta\omega$ in degrees. The incidence angle must be increased for a convex and decreased for a concave sample, respectively, when the beam moves from A to B on the sample. Thus $\Delta\omega$ is negative for a convex and positive for a concave sample. For the measurement a substrate peak is preferred because for a layer peak the lattice parameter could laterally change thus introducing an error. Alternatively, the sample can be illuminated using different apertures in front of the sample, e.g. slits with slit widths $s = 50 \mu\text{m}$ and $s = 1 \text{mm}$ (Fig. 2). The illumination with a parallel beam using the small slit yields the intrinsic width, whereas the illumination with the broad slit, in addition, yields the Bragg peak broadened due to the bending. The width of the illuminated area on the sample is $l = s / \sin \Theta$. From the difference in the halfwidths the radius of curvature can be calculated, i.e., $R_{\text{exp}} = \frac{s}{\sin \Theta_B \Delta\omega}$.

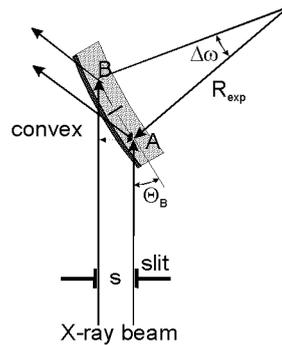


Fig. 2. X-ray method for measuring the radius of curvature of a bent sample.

The radius of wafer curvature for GaN on Si is often around 2 m and less. An example for such a measurement is given in Fig. 3. Without the slit the Si(111) reflection is significantly broadened. In this example a curvature radius of 2.9 m was measured. From *in situ* measurements during MOVPE GaN was found to grow with a tensile stress of about $0.2 \text{ GPa}/\mu\text{m}$ [8]. It should be pointed out that these values were obtained using Stoney's equation [9]:

$$\sigma_f = \frac{E_s t_s^2}{6 t_f R_{\text{exp}}},$$

which does not contain the contribution due to the biaxial stress ($\sim 1/(1 - \nu)$). Thus, assuming a Poisson ratio of 0.23, the internal thermal stress is 30% higher. The origin of the tensile stress at growth temperature was supposed to be correlated with the coalescence of the three-dimensional islands [10]. However, the tensile stress at growth temperature immediately arises at the initial stage of growth before coalescence and remained constant as the film became fully continuous [8]. Thus, further investigation is needed to determine the physical origin of the tensile stress in GaN layers during growth. Cooling to room temperature

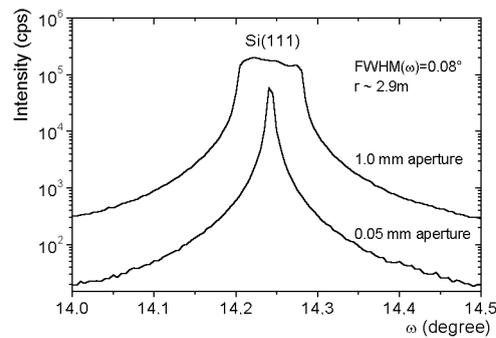


Fig. 3. Determination of stress in GaN/Si by measuring the radius of curvature by X-ray diffraction rocking curves on the Si(111) Bragg reflection.

adds another ≈ 0.7 GPa/ μm , the biggest and certainly the most problematic part. Fu and co-workers showed that the residual stress of GaN on Si depends on the V-III ratio and can be reduced for high V-III ratios [11]. They assume this to originate in a reduced impurity incorporation. Impurities like Si and Mg used for *n*- and *p*-type doping, respectively are reported to strongly enhance the tensile stress of GaN layers. Especially for Si doping around 0.1 GPa/ μm of additional tensile stress is induced for each doping concentration of $1 \times 10^{18} \text{ cm}^{-3}$, e.g. for a high Si-doping of $5 \times 10^{18} \text{ cm}^{-3}$, 0.5 GPa/ μm are added [12].

3. Stress-control

3.1. Insertion of stress-compensating layers

The tensile stress in the GaN layers can be compensated by the insertion of compressive layers. An AlGaIn buffer layer was applied by Ishigawa et al. [13, 14] who obtained crack-free 1 μm thick GaN with an GaN (0002) X-ray rocking curve width of 600 arcsec and narrow 4.2 K PL of the band edge emission of 8.8 meV. The same group recently presented a crack-free LED structure based on such a buffer layer with a relatively bright electroluminescence of 20 μW at 20 mA when compared to other LEDs on Si [15].

Marchand and co-workers [16] used a graded 800 nm thick AlGaIn buffer layer on an AlN seed to induce compressive stress. For a sample with a thin 200 nm GaN cap they induced a compressive stress in the top layer of 0.27 GPa. The 1 μm thick structure exhibits a high dislocation density well above 10^{10} cm^{-2} . The authors assume that a 2-dimensional growth mode of the graded AlGaIn buffer avoids that dislocations bend and annihilate. Based on such a buffer layer they demonstrated a transistor structure.

Growth of 2 μm GaN on Si(111) with and without a step graded AlGaIn buffer on an AlN seed in an ultrahigh vacuum chemical vapor deposition reactor is reported by Kim and co-workers [17]. They observed an improvement of layer quality in X-ray rocking curve FWHM of the GaN(0002) and the asymmetric

GaN(10–12) reflection from 828 arcsec to 720 arcsec and from 1008 arcsec to 864 arcsec, a reduction of the room temperature PL FWHM from 43.5 meV to 30 meV, and a reduction of AFM rms on $20 \times 20 \mu\text{m}^2$ from 41 to 17 nm for the sample without and with the graded AlGaIn buffer, respectively. Also the crack density of the sample with the AlGaIn buffer was significantly reduced.

Stress reduction due to a 15-fold AlGaIn/GaN buffer layer 1.5 μm in total thickness was observed by Dadgar et al. [18]. Here the stress is reduced probably by partial relaxation of the layer after a thickness of approximately 0.9 μm leading to a net compressive stress of the top GaN layer after 2.4 μm but also to cracks. Feltin and co-workers report on a buffer structure consisting of several AlN/GaN superlattices which induce compressive stress sufficient to grow 2.5 μm crack-free GaN on top of it with a biaxial tensile stress of 470 MPa [19–22]. The AlN/GaN superlattice consists of 3 stacks of 10 periods of 3 nm AlN and 4 nm GaN separated by 200 nm GaN. They demonstrated that they can build up enough compressive strain to grow a 2.5 μm thick crack-free GaN layer on top. Also a crack-free LED structure was presented but it shows cracks after processing as can be seen in [19]. This is probably due to the high stress of the sample, which shows a curvature of only 1 m^{-1} . The layers showed X-ray rocking curve widths of 500 arcsec and narrow PL luminescence of 6 meV at 10 K. The dislocation density decreased from $1.5 \times 10^{10} \text{ cm}^{-2}$ for a sample without superlattices to $2.5 \times 10^9 \text{ cm}^{-2}$ for the best uncracked sample with 4 stacks of superlattices.

3.2. Stress control by selective area growth on patterned substrates

Patterning a silicon substrate by etching or masking the substrate or a buffer layer is one way to grow thick crack-free GaN layers. The idea is not to avoid cracks completely but to guide them in the patterned regions, which are equal to the masked part of the Si substrate. As long as the patterned regions are smaller than the average crack density no cracking of the layer grown on Si should occur since the substrate is softer. The simplest way to apply patterning is the deposition of Si_xN_y or SiO_2 directly on the substrate. Since such a layer is amorphous no oriented crystalline seed layer for subsequent growth can be grown on it. Usually, no or only spurious polycrystalline growth is observed on such a mask. The other possibility is etching trenches deep enough to avoid that the layers form a continuous film during growth.

Zamir and co-workers used etched trenches and call this technique lateral confined epitaxy. In their experiments they find that for 700 nm GaN already a field size of $14 \times 14 \mu\text{m}^2$ is the limit for crack-free growth [23]. Such thicknesses are, however no problem to grow crack-free on a whole wafer. Thus it is likely that a poor material quality is the reason for cracks. They also observe an enhancement in PL intensity for smaller sized fields and correlate this with an enhanced quality of the layer [24, 25]. Dadgar and co-workers have demonstrated 2.5 μm thick crack-free GaN layers on $300 \times 300 \text{ mm}^2$ with a similar technique [26].

Honda et al. showed that they can grow crack-free $1.5\ \mu\text{m}$ thick GaN on $200 \times 200\ \mu\text{m}^2$ fields [27]. A growth enhancement at the edge of the fields is observed [27, 28] which depends on the width of the masked region and is caused by mass transport from the masked region. X-ray rocking curve widths of the GaN (0004) reflection for a $1.5\ \mu\text{m}$ thick layer of 388 arcsec and 1130 arcsec and a 77 K PL GaN band edge FWHM of 18.6 meV and 25.8 meV on the $200 \times 200\ \mu\text{m}^2$ fields and for an unstructured layer are obtained, respectively [27].

To efficiently reduce stress AlGaN/GaN multilayers which can be used as Bragg reflectors have been proven to be beneficial [18]. They can relax some stress during growth without forming cracks and in this way reduce the overall stress. On the base of these layers a $3.6\ \mu\text{m}$ thick LED structure on $100 \times 100\ \mu\text{m}^2$ was demonstrated [28]. Despite the total layer thickness of $3.6\ \mu\text{m}$ the stress in the GaN layer was only 0.33 GPa. Since the cracks are propagating in the masked regions between the devices, device separation gets very easy especially for square patterns as preferably used for LED structures. The preferred crystallographic planes for cleaving are along (110) so Si(111) is naturally separated into triangles. Due to the cracks and the stress induced by the GaN fields separation along these natural cleaving planes gets very difficult and the separation of square device structures is simplified.

However, two problems arise with the method of patterning. Due to the tensile stress cracks occur in the Si substrate during growth especially at lowered temperatures as required for InGaN quantum well growth and meltback etching can be initiated from these cracks. Since growth on the mask is strongly suppressed and only enhanced for Al-rich layers, diffusion of GaN onto the growing surface enhances the growth rate at the edge of the device. For thick layers or wide masked regions this can lead to problems in device processing. This effect can be greatly reduced when etched substrates are used.

3.3. Low-temperature AlN interlayers

Amano and co-workers were the first to apply low-temperature AlN (LT-AlN) layers to reduce the defect density of GaN layers [29]. They also served for the growth of crack-free AlGaN layers on GaN on sapphire [30] and can be also used to avoid cracking of GaN on Si [31]. The layers are usually only 10–20 nm in thickness and sufficient to counterbalance thermal tensile stress of approximately $0.7\text{--}1\ \mu\text{m}$ thick GaN while maintaining and usually even improving layer quality. The mechanism leading to a compensation of tensile thermal stress has long been unclear and a first study now enlightens the mechanism, which can be shortly described as a decoupling of the GaN layers above and below an LT-AlN layer [32]. AlN interlayers deposited at different temperatures show that the deposition temperature is the most important parameter for a compensation of tensile thermal stress. Reciprocal X-ray diffraction measurements of a multilayer sample clearly show that high temperature deposited AlN grows pseudomorphically on

GaN as well as the following GaN or AlGaIn layer on top of the AlN-interlayer, i.e. all layers have the same a -lattice. At lower growth temperatures the LT-AlN layer grows incoherently on the underlying GaN layer whereby the epitaxial symmetry is maintained, i.e. the c - and a -axes orientations are maintained and even improved by the LT-AlN clearly visible in a reduction of rocking curve widths for the GaN(0002) reflection from 720 arcsec to 600 arcsec and the asymmetric GaN(20-24) reflection from 270 arcsec to 65 arcsec for a 1.3 μm thick GaN layer with and without LT-AlN interlayers, respectively [33]. The GaN or AlGaIn layer grown on top of the LT-AlN layer is partially compressively stressed which counterbalances the stress when grown on Si. As an example in Fig. 4 the X-ray diffraction

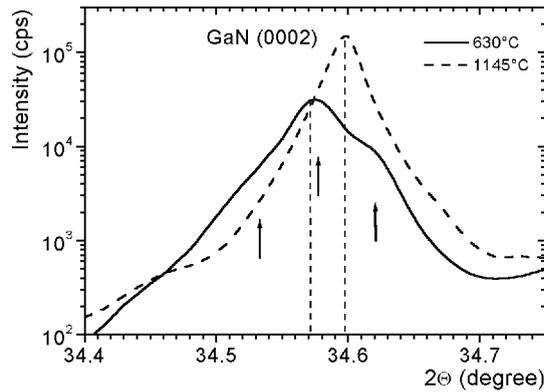


Fig. 4. θ - 2θ scan around the GaN(0002) reflection of two GaN samples on Si with two AlN-interlayers grown at low (630°C) and high (1145°C) temperatures. The low-temperature interlayers decouple the GaN into three parts of different stress.

(0002) θ - 2θ pattern of a thick GaN sample with two LT-AlN interlayers grown at 1145°C and 630°C is shown. For the sample with the high temperature interlayers a single Gaussian diffraction peak is observed indicating the same c -lattice parameter for the whole stack, whereas for the sample with the LT-AlN interlayer a splitting in three components is visible, i.e. the three GaN layers are decoupled from each other. For thick GaN layers with multiple LT-AlN layers a bowing of the wafer can be observed. If the bowing gets too strong a poor thermal contact with the substrate holder occurs resulting in an inhomogeneous layer quality. Thus an accurate balancing of the GaN layer thicknesses is important to maintain a low curvature even during growth. For this purpose an *in situ* stress measurement e.g. a multi-beam-optical-stress-sensor (MOSS) which directly measures the wafer curvature during growth is helpful [34, 35].

4. Crack-free light-emitting devices on silicon

Using the patterning technique Dadgar et al. [28] fabricated a crack-free $3.6 \mu\text{m}$ thick $100 \times 100 \mu\text{m}^2$ LED structure. The diode showed bright electroluminescence with an onset at 3.2 V and a series resistance of 350Ω .

Zhang and co-workers presented a crack-free LED applying an AlGaIn buffer layer and keeping the total thickness of the device low ($\approx 1 \mu\text{m}$) [36]. The thick AlN (120 nm) AlGaIn (380 nm) buffer layer [13, 14] prevents cracking of the subsequently grown film by inducing compressive stress during growth. The output power is 23 and $19.4 \mu\text{W}$ at 20 mA and 506 nm with 8 V and 16 V necessary to drive this current for top and vertically contacted LEDs. After this the same group presented a slightly improved LED based on the same buffer layer but with thicker GaN layers and a total thickness of $\approx 1.5 \mu\text{m}$ [15]. Despite the relatively thick, high band gap buffer layer an improvement of the LED was achieved and a relatively low series resistance of 100Ω obtained for vertically contacted LEDs. This is one of the best values reported on Si(111). Light output power is $20 \mu\text{W}$ at 505 nm and 20 mA (7 V) current. They performed lifetime testing over 500 hours and could not observe any degradation of the device.

Felton et al. grew a thick crack-free LED structure with the AlN/GaN superlattice buffer layer described above [19]. While the structure is reported to be crack-free, processing obviously induced cracks. Introducing LT-AlN interlayers for strain engineering and an Si_xN_y *in situ* mask Dadgar and co-workers succeeded in the growth of a crack-free $2.8 \mu\text{m}$ thick LED structure on a 2" Si(111) wafer [37]. In addition to the LT-interlayers, the structure contained a silicon nitride *in situ* mask as first introduced by Lahrèche et al. [38] for the growth of GaN on sapphire and first applied by Hageman et al. to the growth of GaN on Si [39]. The light output power of $420 \mu\text{W}$ at 20 mA and 498 nm is already sufficient for indicator lights. The resistivity could be reduced to 40Ω and is the best value reported so far. By using the *in situ* mask the dislocation density could be drastically reduced by an order of magnitude from $\approx 10^{10} \text{cm}^{-2}$ to $\approx 10^9 \text{cm}^{-2}$ resulting in an improved cathodoluminescence intensity by a factor of 5 [40]. The impact of the *in situ* mask is schematically shown in Fig. 5. After the insertion of the

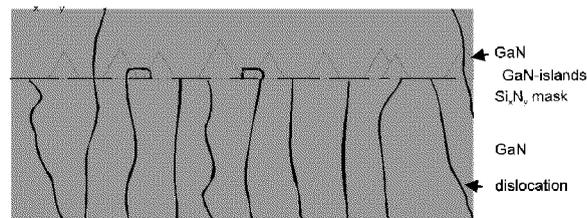


Fig. 5. Scheme of dislocation termination by a silicon nitride *in situ* mask.

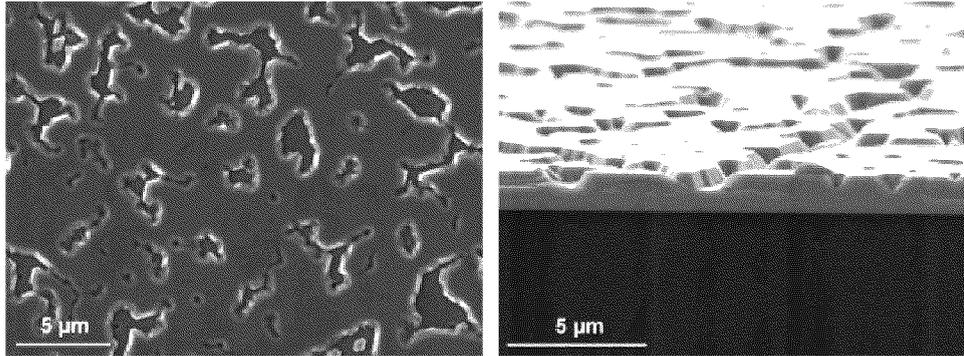


Fig. 6. Impact of a silicon nitride mask on the growth of GaN. Growth proceeds from openings in the mask in an ELOG-like manner; top view (left) and side view (right).

mask the GaN growth proceeds from openings in mask in an epitaxial lateral overgrowth-like (ELOG-like) manner (Fig. 6). In order to avoid the accumulation of a critical stress thickness of $\approx 1 \mu\text{m}$ a fast coalescence is necessary, which could be achieved by properly adjusting the V–III ratio.

5. Outlook

GaN growth on Si has developed rapidly in the last few years. The main problem — thermal mismatch — has been solved by several concepts for device-relevant thicknesses and the layer quality is sufficiently good for manufacturing LED and FET devices. For laser devices on Si a significant reduction in dislocation density is needed. Therefore methods as ELOG, pendeo and cantilever epitaxy must be combined with stress reducing layers to achieve uncracked films with a low dislocation density. Even for the growth on sapphire and SiC the problems with high dislocation densities and low lifetime are severe and at the moment only few groups succeeded in the growth of laser devices with a cw-lifetime of more than one hour. If no large homoepitaxial GaN substrates are available in the near future, Si substrates will certainly play a role in production of FETs and LEDs and maybe even for laser devices especially since substrate removal is very simple.

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