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Micro-optical and Optoelectronic Components for Optical Interconnection Applications

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The advances in the design and fabrication of microlaser arrays, photodetectors, and free-space optical interconnection elements have driven the creation of ever more "real world" demonstrator systems. In this paper we review the progress made to date on two separate demonstrator projects which have been assembled at Heriot–Watt University. We shall describe some of the enabling technologies used in the creation of these systems and outline the potential for scaling the architectures described up to sizes where the computational advantages of the optics-in-computing paradigm become highly attractive.

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1. Introduction

The increasing array sizes of optoelectronic devices in conjunction with the decreasing power requirements of the individual devices are driving the development of optics-in-computing system demonstrators. The purpose of these systems is to show the suitability of free-space interconnected optoelectronics for deployment into the general communications environment. In particular, microlaser arrays, in conjunction with diffractive optical elements, appear to offer the maximum flexibility in the problems they can address.

This paper describes two free-space systems based around vertical-cavity surface-emitting laser (VCSEL) arrays. The first, an analog system, is designed to perform optimization on a two-dimensional data set. The second is the implementation of a 1 Tbit/s aggregate bandwidth digital crossbar switch. The individual optoelectronic modules that make up each of these systems are characterized and some of the techniques used in the assembly of the complete systems are outlined.

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2. The Hopfield network system demonstrator

The physical implementation of the high bandwidth parallel processing architecture commonly known as a "neural network" [1] requires two distinct hardware modules, the array(s) of thresholding processors (neurons) and the inter-processor connections (weights). The inherent flexibility of diffraction-based free-space optics allows any arbitrary topology of inter-processor connection to be constructed at no extra cost in terms of system size; i.e. a system with twenty connections per neuron will occupy the same space as a system with two hundred connections per neuron. The precise form taken by the interconnection topology depends upon the type of problem being addressed. It should be noted that in this section the neural architecture under discussion is one where the interconnection topology is fixed and can be determined analytically before operation. Adaptive architectures, such as the error backpropagation multi-layer perceptron or the adaptive resonance theory network, lie outwith the scope of this paper.

The system demonstrator described in this section is based around a Hopfield-type neural network [2] and is designed to perform a crossbar switch throughput optimization. Figure 1 shows a schematic of the system in which the network

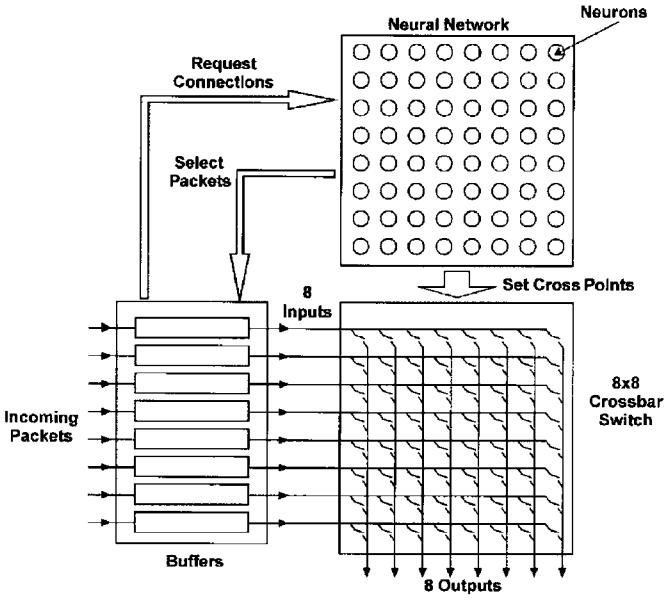

Fig. 1. The crossbar switch hardware incorporating the Hopfield network switch controller.

operates. Incoming data packets are stored in the input buffers and the header of each incoming packet is decoded by the queue manager for that input line to generate the appropriate interconnection request. When each queue manager receives a packet header from its input line, it examines the destination address to determine which output line that packet wishes to use. It then updates its internally stored request vector by setting the bit of the appropriate column. The request vectors of all queue managers are supplied to the Hopfield neural network, which has one neuron corresponding to each cross point in the crossbar switch. The neural network uses the combined request vectors as its initial state and computes an optimal configuration for the crossbar switch. The resulting configuration vector is returned to each queue manager, and those cross points selected by the Hopfield network are then closed. Each queue manager transmits a single packet as selected by the returned configuration vector through the crossbar switch to the appropriate output and updates its row request vector by clearing the bit of the selected column if no more packets for that output remain. This process continues in a cycle where new packets are being received while queued packets are being transmitted. The throughput of the switch is said to be optimized if the number of packets selected for transmission by the Hopfield network on any one switch cycle is equal to $\min(N_{\mathrm{I}}, N_{\mathrm{O}})$.

The Hopfield neural network, which controls the setting of the crossbar switch as described above, is implemented using free-space optical interconnections in conjunction with arrays of optoelectronic devices. These optoelectronic devices provide the electronic-optic and optic-electronic interfaces to the diffractive optical element (DOE) based free-space interconnection. The electronic-optic interface consists of an 8×8 array of VCSELs with appropriate analogue ASIC VLSI drivers. The optic-electronic interface is an off-the-shelf Si photodetector array with a transimpedance amplifier to produce the correct voltage levels for application to the neurons. The neurons themselves are implemented electronically using Texas Instruments digital signal processors (DSP), which each supply the functionality for 16 neurons. Figure 2 shows a schematic of the optical layout of the Hopfield network and a photograph of the optomechanical baseplate used in the system demonstrator.

The DOE provides the inhibitory interconnections between the neurons. Using standard optimization techniques [3], high efficiency ($> 70\%$), low reconstruction error ($< 1\%$) non-local interconnections can be designed and fabricated [4] using conventional VLSI techniques. The interconnection required for the crossbar switch throughput optimization problem is shown in Fig. 3.

The diffractive optical element was designed using a combination of an iterative Fourier transform algorithm (IFTA) and a closed-form trapezoidal algorithm [3]. In general, these standard design methods allow the creation of DOEs with efficiencies of $> 70\%$ and reconstruction errors of $< 1\%$. However, due to the restrictions placed upon the DOE period by the optical system, a reduction in the

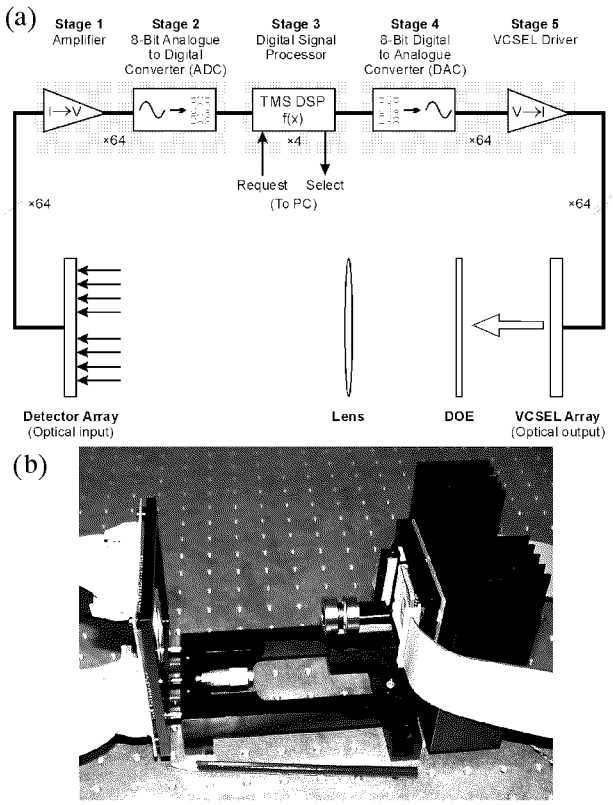

Fig. 2. Optical layout of Hopfield network demonstrator: (a) electronic system, (b) optical system.

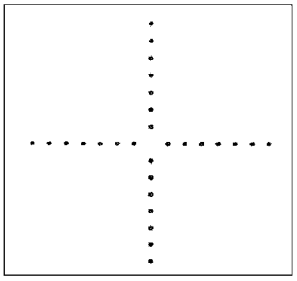

Fig. 3. Inhibition pattern required by Hopfield network.

overall efficiency of the DOE to 50% was required to ensure that the nonuniformity was of an acceptable level. The period of the DOE is given by

$$T = \frac{nf\lambda}{s}, \tag{1}$$

where n is the number of orders between collinear "on" diffraction orders, f and λ

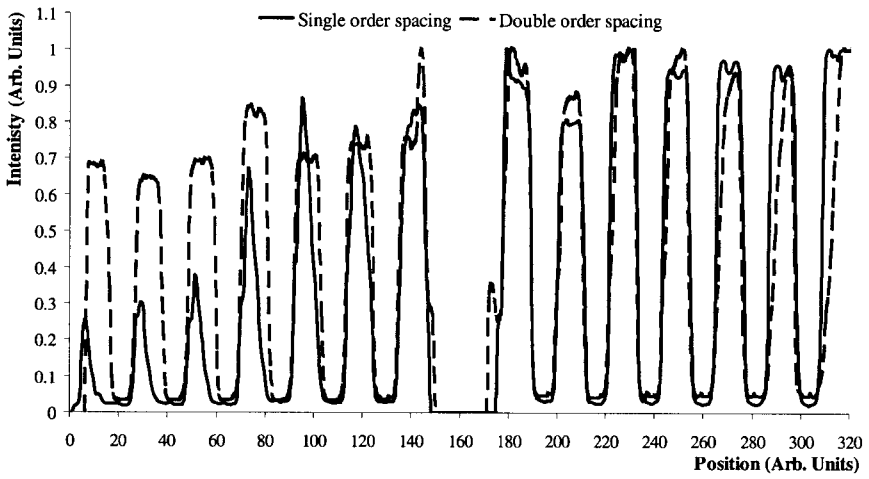

Fig. 4. Cross-section through inhibition interconnection DOE output.

are the focal length and wavelength respectively and s is the separation between "on" diffraction orders. Figure 4 shows the output from two different inhibition DOEs, the first designed with the collinear spacing between the diffraction orders set at one diffraction order and the second with the collinear spacing set to two diffraction orders.

It can be seen from Fig. 4 that the larger period produced by the double order spacing has improved the overall uniformity of the element. This improvement in final uniformity is due to the larger minimum feature size of the double order spacing element and the commensurate improvement in the photolithographic transfer of the phase profile onto the glass substrate.

The VCSEL arrays used in the Hopfield network demonstrator are 8×8 arrays (250 μm pitch) supplied by Avalon Photonics as shown in Fig. 5.

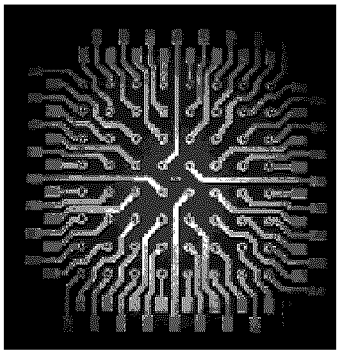

Fig. 5. 8×8 VCSEL array used in Hopfield network demonstrator.

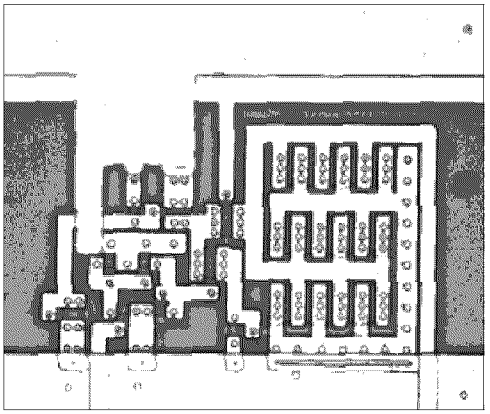

Fig. 6. Analogue CMOS current driver circuit.

The original microlasers used in the demonstrator [5] emit in the near infrared ($\lambda = 960$ nm) at a divergence angle of 12° FWHM. The average threshold current of the microlasers is 2.65 mA and the average peak power-conversion-efficiency is 6.3%. The ASIC CMOS current driver circuits shown in Fig. 6 supply a maximum current of 3.5 mA at 2 V producing an optical output of 200 μW.

The optical output in each channel can be improved by the use of oxide-confined (OC) VCSELs [6], which exhibit a significantly higher conversion efficiency, lower threshold current and improved operating lifetime. This last factor has become significant during the assembly of this demonstrator as the original (non-OC) VCSEL array ceased laser operation during testing of the VCSEL driver circuits. The average threshold current of the OC VCSELs is 0.74 mA with an average peak power-conversion-efficiency of 14.3%. Simulations of the current driver circuits with these VCSELs have demonstrated that a maximum current of 4 mA at 2 V is achievable, corresponding to an optical output of 1 mW. The maximum optical power incident upon a single photodetector from one VCSEL is equal to

$$P_{\text{detector}} = \frac{\eta P_{\text{VCSEL}}}{4(N-1)},$$

where η is the overall efficiency of the DOE (0.5 in this case), N is the number of input/output channels in the system and P_{VCSEL} is the maximum optical output from the VCSEL. For the demonstrator system described here, the maximum power per detector is 3.57 μW for the non-OC VCSELs and 17.86 μW for the OC VCSELs. The photodetector array, which is an off-the-shelf Si array, has responsivity at 960 nm of 0.35 A/W, producing a photocurrent of 1.25 μA with the non-OC VCSELs and 6.25 μA with the OC VCSELs. A discrete component amplifier has been designed to convert this photocurrent into a voltage for application to the DSP-based neurons. The amplification factor of this amplifier was determined by

calculating the maximum photocurrent that can be generated by one photodetector and equating that photocurrent with a voltage swing of 1 V. The total number of VCSELs that can communicate with a single photodetector is $2(N-1)$ giving a maximum generated photocurrent of 17.5 μA/87.5 μA (non-OC/OC VCSEL). Figure 7 shows the voltage modulation supplied to a single DSP from a sinusoidal input wave form at frequencies up to 10 MHz.

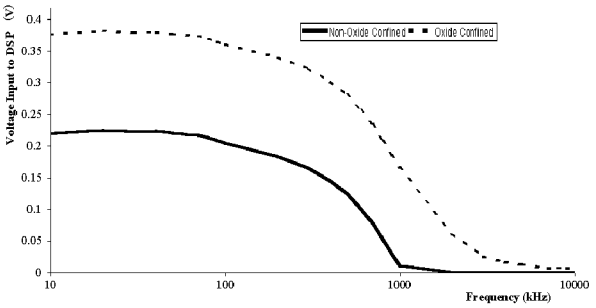

Fig. 7. Frequency response of optoelectronic system.

The lower cut-off frequency for non-OC VCSELs observed in Fig. 7 is due to their relatively high threshold current. It is anticipated that the switch to the lower threshold current oxide-confined VCSELs will allow the Hopfield network demonstrator to be operated at an iteration frequency of 2–3 MHz.

3. Hopfield network demonstrator simulations

Although the demonstrator hardware outlined in the preceding section is non-operational at present, the individual modules (i.e. VCSELs and drivers, photodetector array, optical system and the DSPs) have been sufficiently characterized to permit accurate simulations of the convergence behavior of the network with respect to different operational parameters. The parameters studied in this paper are the tolerance of the network to optical system non-uniformity and the relative efficiency of different VCSEL driver operation modes.

The DOE nonuniformity or reconstruction error observed in Fig. 4 is a system parameter of critical importance to the successful operation of the Hopfield network. If the DOE nonuniformity rises above some critical level the solutions provided by the network will be sub-optimal, i.e. the average number of packets switched through the crossbar on any network cycle will be less than N. This is demonstrated by Fig. 8 which shows the average number of packets switched through an 8×8 crossbar for increasing levels of DOE nonuniformity.

It can be seen that up to a certain level the Hopfield network is immune to increasing DOE nonuniformity, however DOE nonuniformity above that critical level produces a gradual degradation in network performance. For the 8×8

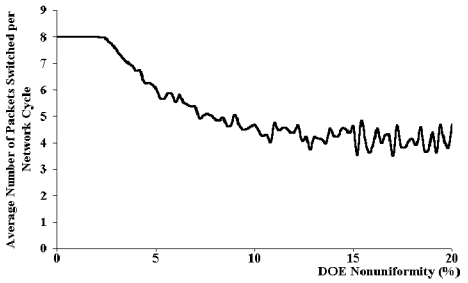

Fig. 8. Degradation of Hopfield network operation with increasing DOE nonuniformity.

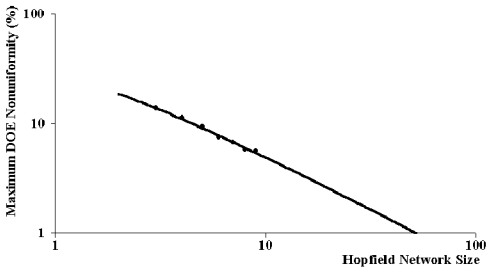

Fig. 9. Maximum DOE nonuniformity for different network sizes.

Hopfield network, this critical DOE nonuniformity level is 2%. Typically, DOEs have a design nonuniformity, i.e. the nonuniformity of the idealized design before fabrication, of $\approx 0.1\%$. The fabrication processes add nonuniformity to this unavoidable design nonuniformity. The primary mechanisms which produce this fabrication nonuniformity are etch depth inaccuracies and the rounding of sharp features during photolithographic copying. The amount of nonuniformity added during the in-house fabrication process is of the order of 1% per mask level. By simulating different network sizes, as shown in Fig. 9, the maximum size of network that can be implemented using a DOE with 1% nonuniformity can be determined.

For the optoelectronic system presented in this paper the maximum network size which can be implemented using the currently available DOE fabrication technology is 52×52.

The VCSEL array can be driven either digitally, where the VCSEL is switched on above some arbitrary threshold voltage, or analogue, where the VCSEL output is allowed to increase monotonically between a minimum voltage and some predefined maximum value. Figure 10 shows the number of iterations required for the network to converge to a steady state for different network sizes.

It can be seen that the digitally driven network displays better scalability than the analogue network. This better scalability is due to the behavior of the analogue network in the gently sloping central region of the neuron response function. If the neurons are initialized in this region then, for two networks of different

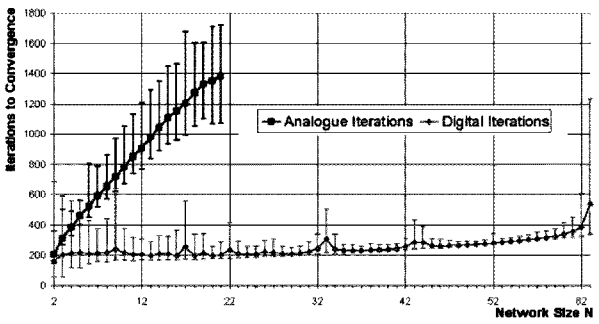

Fig. 10. Comparison of number of iterations required for convergence between digitally driven network and analogue driven network.

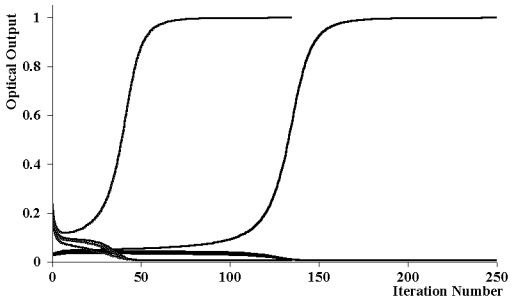

Fig. 11. Dynamic operation of 4×4 and 8×8 Hopfield network.

sizes, it will take correspondingly longer for any significant gap to open between the neurons of the larger network than between those of the smaller network. This is shown in Fig. 11, for two 1D networks containing 5 and 10 neurons respectively. The larger network takes longer to reach a decision point although this can be compensated for by increasing the slope of the neuron response function. Digitally thresholding the neurons is equivalent to an analogue thresholding function with infinite slope.

4. The smart-pixel optoelectronic crossbar (SPOEC) demonstrator

The second demonstrator system [7] considered in this paper is a packet--switched optoelectronic matrix–matrix crossbar based around an InGaAs detector/modulator smart-pixel, where conventional Si-based electronics are combined with optoelectronic devices by means of flip-chip bonding. The system was designed to demonstrate the feasibility of a > 1 Tbit/s aggregate bandwidth switch using currently available optoelectronic technology. Sixty four electrical signals are converted into optical signals by an electrically addressed 8×8 VCSEL array. Each of the 64 optical outputs from the array are themselves fanned out 64 times

by an 8 × 8 fan-out diffractive optical element (DOE). The resulting set of 4096 optical signals is relayed to a hybrid InGaAs/Si OE-VLSI chip which is partitioned into 64 blocks or "super-pixels". Each super-pixel receives the full set of 64 optical input signals and converts these into electrical signals that are electrically routed by the Si-based electronics. The unique output from each super-pixel, which represents the one signal selected from the original set of 64, is converted back into an optical output by means of a differential pair of multiple-quantum-well modulators. The system is designed as a packet switch with the routing chip configured by the packet header. Figure 12 is a schematic of the layout of the system showing the optical pathways used for the data-in (at $\lambda = 960$ nm) and data-out (at $\lambda = 1047$ nm) channels.

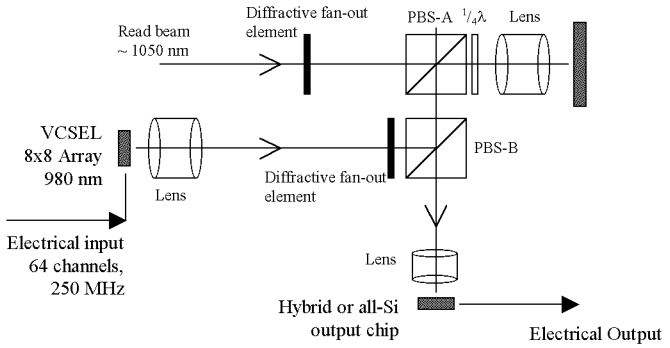

Fig. 12. The smart-pixel optoelectronic crossbar demonstrator.

The diffractive optical elements used in the SPOEC demonstrator are an 8×8 (DOE1) and an 8 × 16 (DOE2) binary even-orders-missing (EOM) fan-out [8]. The EOM geometry is used because it gives excellent zeroth diffraction order suppression and significantly speeds up the DOE optimization procedure.

Figure 13 shows the phase profile and simulated output of the 8 × 8 fan-out. It has a period of 72 μm with a minimum feature size of 2 μm and the diffraction efficiency of the element is 71% with a reconstruction error of $< 0.5\%$.

The VCSELs used to supply the optical input data to the system, which are of the same type as those used in the Hopfield network demonstrator, have a large beam divergence ($\approx 20°$) due to the small size of the laser cavity. This large divergence is reduced, by means of a refractive microlens array, to keep the design tolerances on the bulk optical elements within reasonable bounds. The VCSEL outputs are not collimated to ensure that a sufficient number of periods of the DOE (typically 3 × 3) are illuminated to give a uniform fan-out pattern at the smart-pixel array. Figure 14 shows the patented method [9] used to ensure that each microlens is centered on the appropriate VCSEL. Reflective Fresnel zone plates are placed around the VCSEL array during fabrication and rings are etched

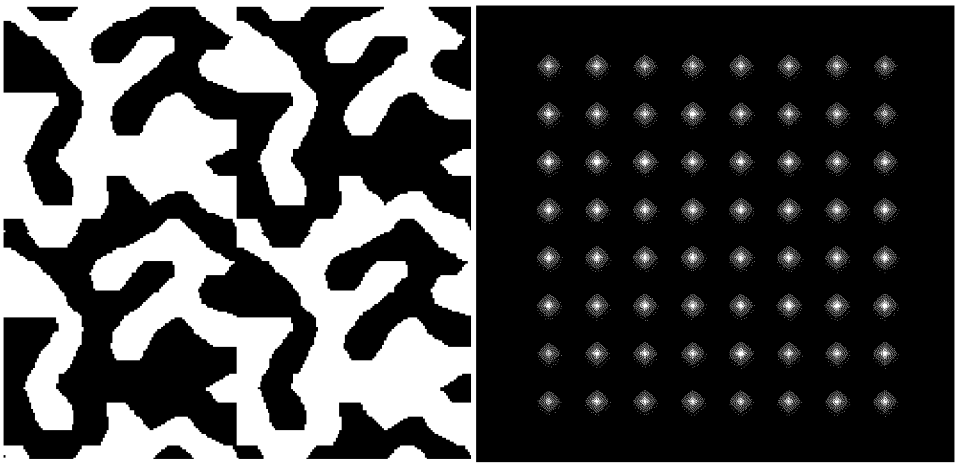

Fig. 13. 8×8 binary fan-out phase profile and DOE output.

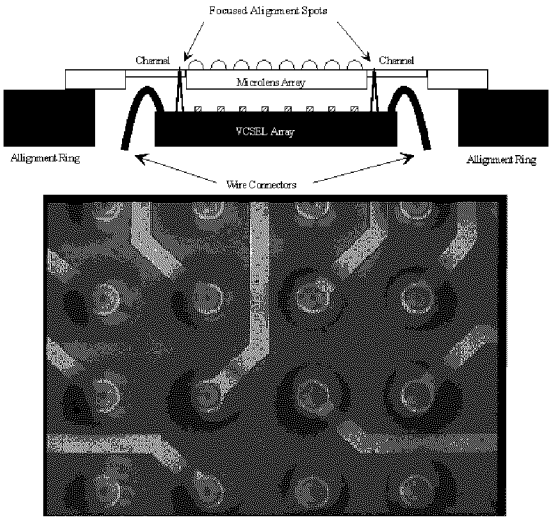

Fig. 14. VCSEL-microlens alignment technique and photograph of VCSELs imaged through microlenses.

onto the microlens array in positions corresponding to the optical axes of the zone plates. During assembly of the hybrid VCSEL/microlens array, the reflective zone plates are illuminated and once each of the rings on the microlens array has a focussed spot in it, the arrays are aligned with each other. The VCSEL–lens separation is controlled by means of a plastic alignment ring of the correct thickness being placed around the VCSEL array. This also provides a convenient platform for securing the microlens array to the VCSEL array.

The effect of the microlens on the VCSEL emission can be seen in Fig. 15.

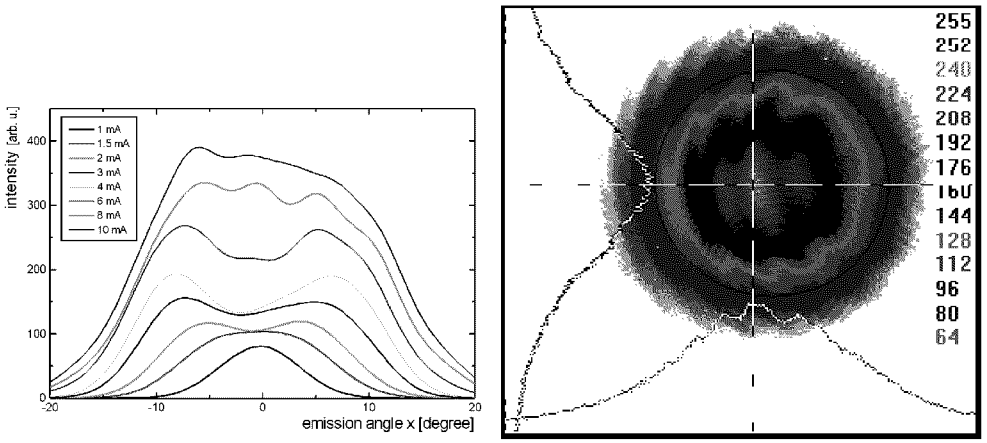

Fig. 15. Angular divergence of VCSEL without microlens and with microlens.

The graph on the left is the divergence of an oxide-confined VCSEL in the absence of a microlens where the FWHM divergence of the VCSEL operating at 6 mA is about 20°. The figure on the right shows the profile of the same VCSEL after passing through an $f/8$ microlens of focal length ≈ 1 mm.

The reduction in the FWHM divergence angle of the OC VCSEL is approximately a factor of 3 (from a divergence of $\approx 20°$ to $\approx 7.5°$).

The fully assembled SPOEC demonstrator has been shown [10] to be capable of correctly routing data through the crossbar for a single channel. The maximum routing frequency achieved to date is 50 Mbit/s for the system operating with fully fanned out VCSEL signals and 250 Mbit/s for the system operating without VCSEL fan-out. With the fully fanned out VCSEL signals the calculated aggregate bandwidth of the crossbar is 0.2 Tbit/s. A more accurate measure of the total aggregate bandwidth of the crossbar switch will be known once the fully parallel operation of the system has been tested.

5. Summary and conclusions

This paper has outlined the development of two free-space optoelectronic optics-in-computing system demonstrators, which, although at present not competitive with conventional electronics, show the power and flexibility of the enabling technologies.

The scalability of both architectures presented in this paper is limited by the VCSEL array size which, at present, is only 8×8 although in principle 16×16 (and 32×32) are well within the capabilities of current fabrication technologies. The use of smart-pixels, in the case of the SPOEC system, simplifies the supply of power to the optoelectronic devices as well as reducing any bandwidth overheads from signal transfer from the optical domain to the electronic. In addition, it

gives optoelectronic systems access to the speed and gate density improvements whose adherence to Moore's law has given conventional microelectronic systems. Diffractive optical elements which produce highly uniform arrays of 256×256 spots have been fabricated using standard 2 μm VLSI fabrication techniques and once smaller feature size VLSI processes are employed in DOE fabrication, significantly larger elements should be feasible. The fabrication of refractive microlens arrays, which utilizes thermal reflow of photoresist, allows arbitrarily large arrays to be fabricated using the current technology.

Acknowledgments

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